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MARCH 1
Issue 5/2007
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NEW

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Howard Johnson's "Signal Integrity": OFC madness Pg 30

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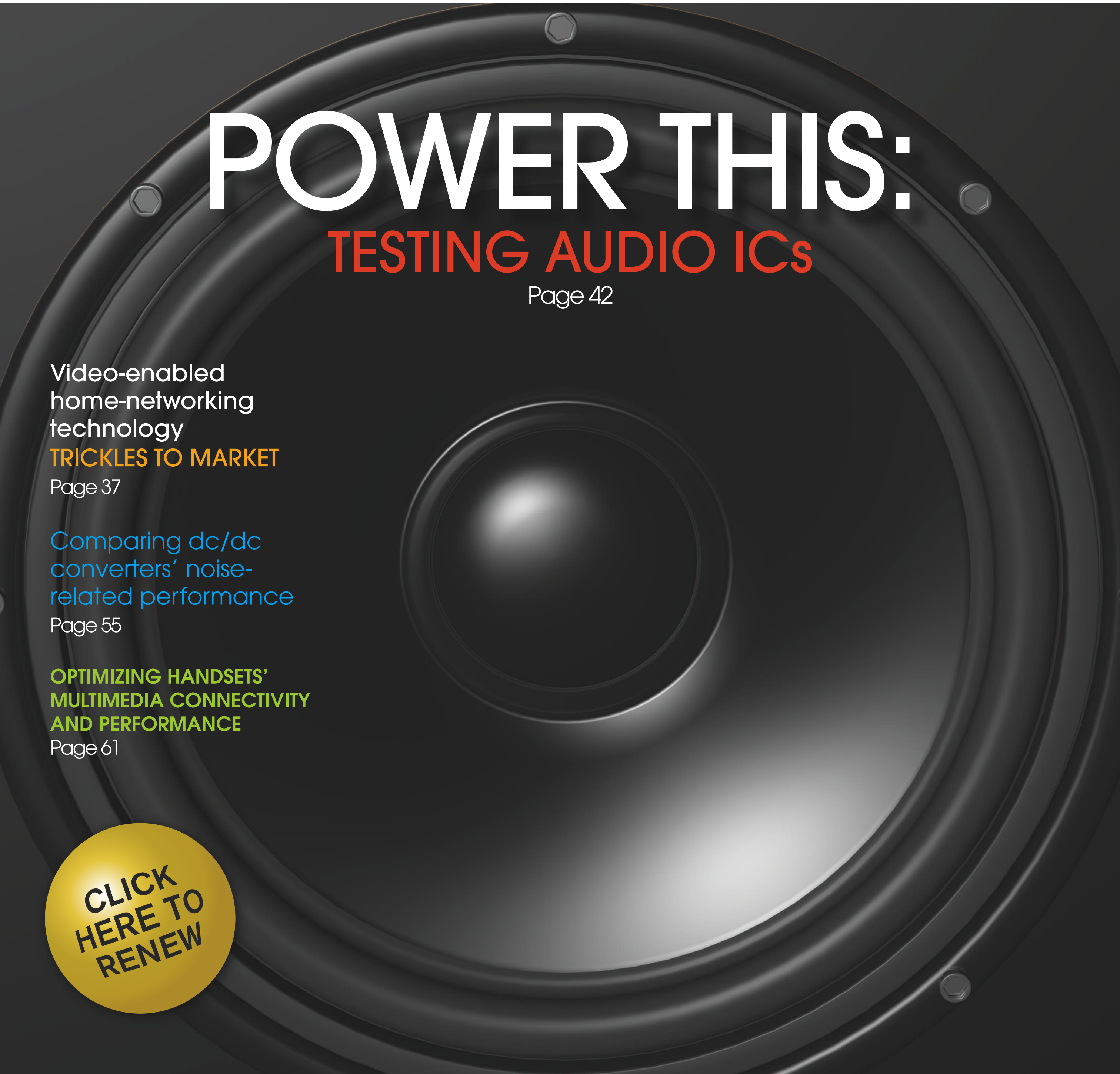

POWER THIS:

TESTING AUDIO ICs

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Comparing dc/dc converters' noise-related performance
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OPTIMIZING HANDSETS' MULTIMEDIA CONNECTIVITY AND PERFORMANCE
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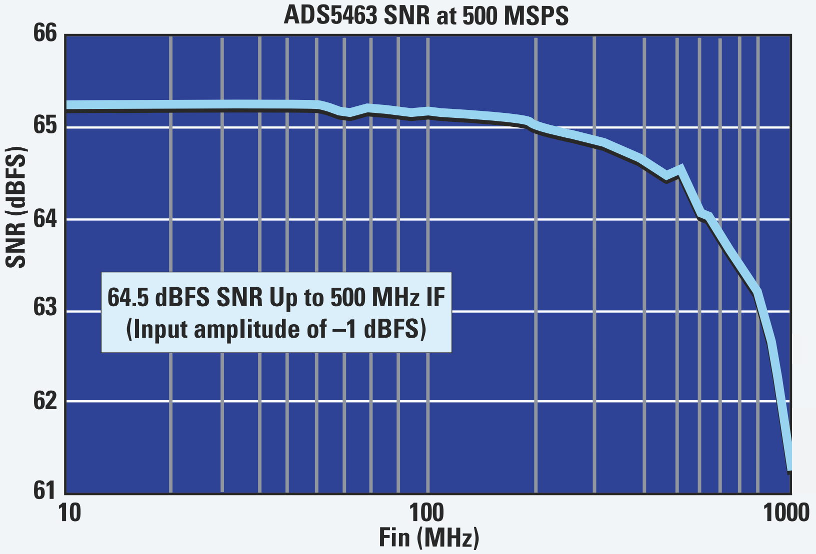
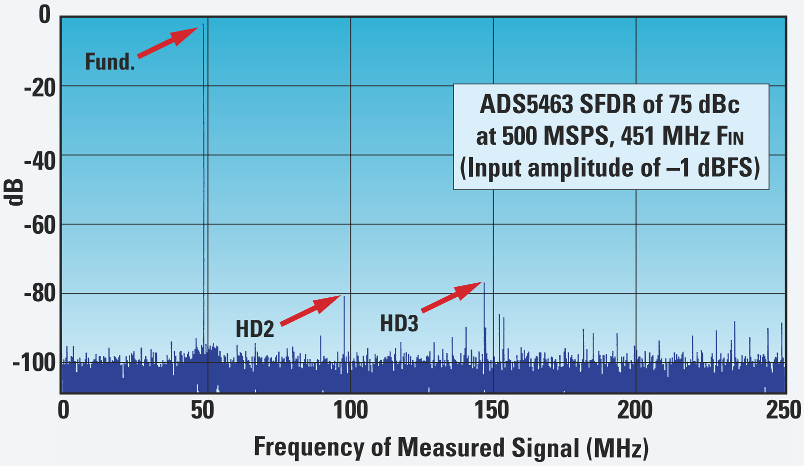
DATA CONVERTERS

12-Bit, 500 MSPS ADC





▶ Applications

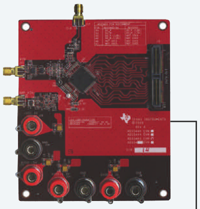
- Power amplifier linearization
- Multi-carrier receivers
- Software defined radio
- Radar and advanced imaging
- Test and measurement

▶ Features

- 12-bit resolution, 10.5 ENOB
- 2 GHz input bandwidth
- Space saving package size: 80-pin TQFP (14mm x 14mm)
- Differential input: 2.2 V_{PP}
- LVDS outputs with simplified data capture
- Total power dissipation: 2.25W
- Ind. temp: ADS5463 –40° C to +85° C
- Mil. temp: ADS5463-EP, QMLV –55° C to +125° C
- Pin-compatible with 13-bit, 210 MSPS ADS5440 and 13-bit, 250 MSPS ADS5444
- Recommended amplifiers: THS9000, THS9001, THS4304, THS4509, THS4511
- In production now: Priced at $125 in 1k units (Industrial temp. only)

The 12-bit, 500 MSPS **ADS5463** from Texas Instruments delivers best-in-class performance with greater than 75 dBc SFDR and 64.5 dBFS SNR for input frequencies through 450MHz. This new ADC benefits the most demanding amplifier linearization, communications, radar, imaging, test and measurement applications – all in a 14mm x 14mm 80-pin TQFP package. The ADS5463 is part of a pin-compatible family of products that include TI's 13-bit 250/210MSPS ADS5444 and ADS5440 ADCs.

For Evaluation
Modules,
Samples and
Technical
Information



www.ti.com/ads5463 ◦ 800.477.8924, ext. 13476

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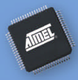

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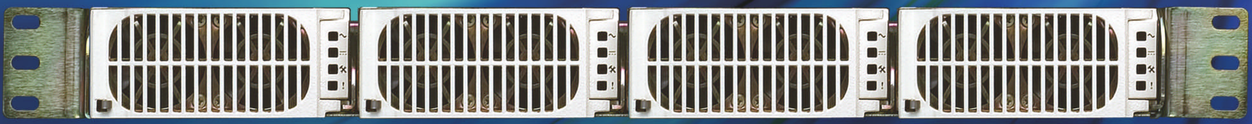
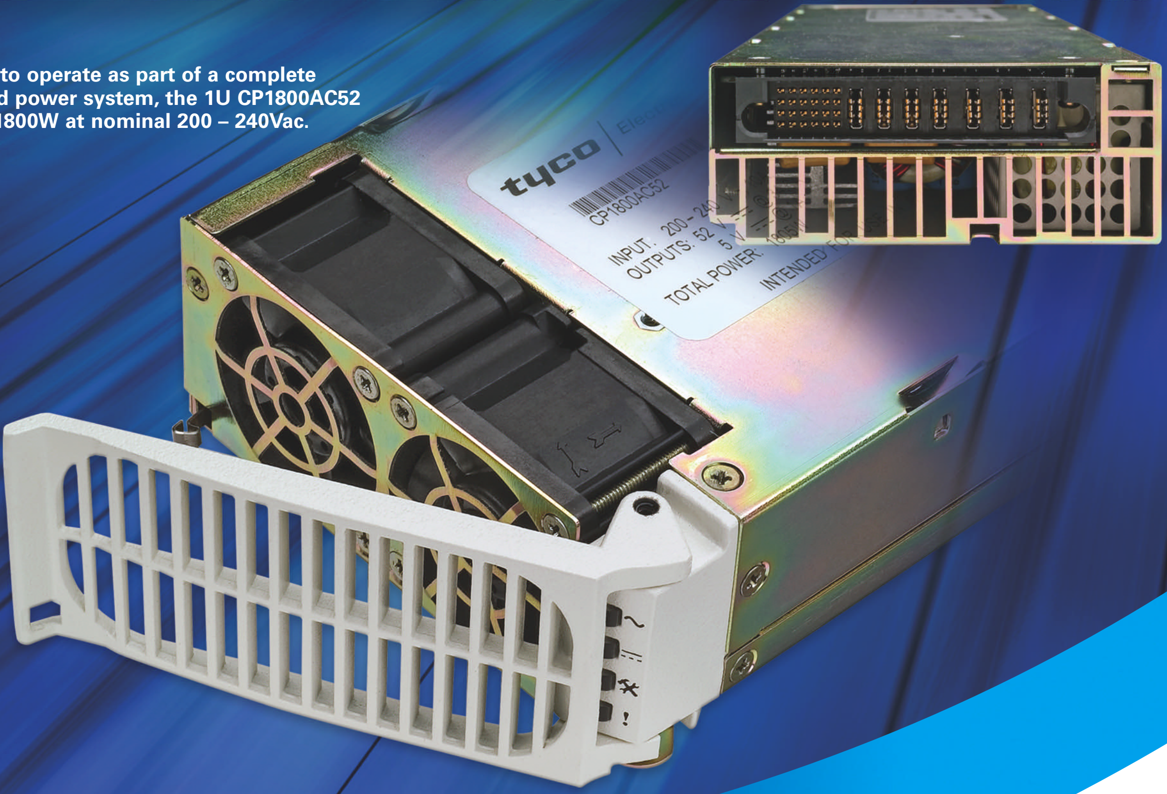
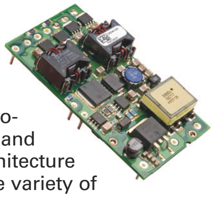


Designed to operate as part of a complete distributed power system, the 1U CP1800AC52 provides 1800W at nominal 200 – 240Vac.





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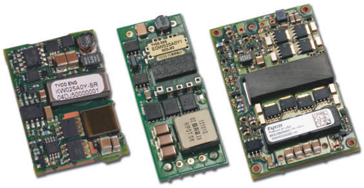

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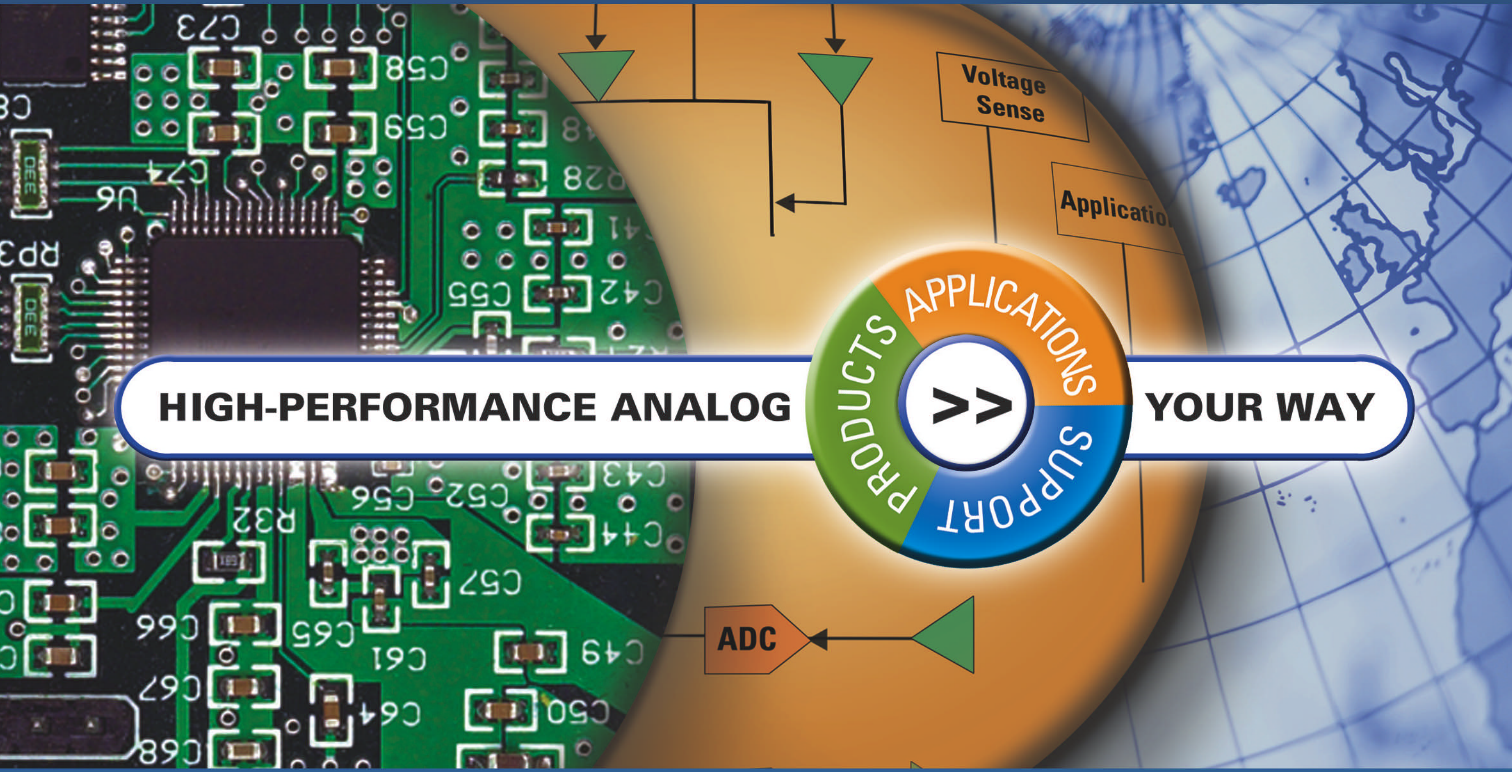

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- Audio ADCs
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- Delta-Sigma DACs
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- Audio SRCs
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- ISM Band
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OPA333	**Lowest power, zero-drift op amp:** 2µA offset, 17µA current, SC70 and SOT23 packages
ADS8422	**Fastest 16-bit SAR ADC (4MSPS)** 2LSB INL, 92.5dB SNR
ADS5546	**Fastest 14-bit ADC (190MSPS)** 73.2 SNR at 70MHz IF; 84dBc SFDR at 70MHz IF; 1.1W power
ISO721	**High-speed digital isolator:** 4000V (peak) isolation; signaling rate of 0-150Mbps; high electromagnetic immunity; low input current requirement; failsafe output
TAS5261	**PurePath Digital™ amplifier** capable of driving more than 300W
TPS63000	**96% efficient buck-boost converter** with up to 28% greater run-time; 3 x 3 mm^2 QFN package
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Application Knowledge

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- Security
- Video & Imaging
- Voice
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Resolution	Speed Range	1 Channel	2 Channel	4 Channel	8 Channel Latest Release!
8 bit	50 KSPS to 200 KSPS	ADC081S021	ADC082S021	ADC084S021	ADC088S022
	200 KSPS to 500 KSPS	ADC081S051	ADC082S051	ADC084S051	ADC088S052
	500 KSPS to 1 MSPS	ADC081S101	ADC082S101	ADC084S101	ADC088S102
10 bit	50 KSPS to 200 KSPS	ADC101S021	ADC102S021	ADC104S021	ADC108S022
	200 KSPS to 500 KSPS	ADC101S051	ADC102S051	ADC104S051	ADC108S052
	500 KSPS to 1 MSPS	ADC101S101	ADC102S101	ADC104S101	ADC108S102
12 bit	50 KSPS to 200 KSPS	ADC121S021	ADC122S021	ADC124S021	ADC128S022
	200 KSPS to 500 KSPS	ADC121S051	ADC122S051	ADC124S051	ADC128S052
	500 KSPS to 1 MSPS	ADC121S101	ADC122S101	ADC124S101	ADC128S102
Packaging		SOT23-6/LLP-6	MSOP-8	MSOP-10	TSSOP-16

Drop-in replaceable across resolution and speed

ADC121S101 Product Features (typical)

- Speed range: 500 KSPS to 1 MSPS
- Integral non-linearity (INL): ±0.4 LSB
- Differential non-linearity (DNL): ±0.5 LSB
- Signal-to-noise ratio (SNR): 72.5 dB
- Signal-to-noise and distortion ratio (SINAD): 72 dB
- Spurious free dynamic range (SFDR): 82 dB
- Power consumption: 2 mW at 3V
- Supply voltage: 2.7 to 5.25V

Family Benefits

- Guaranteed performance over speed
- Pin and function compatible family
- Excellent static and dynamic performance
- Extremely low power
- Miniature packages reduce board space


SOT23-6


LLP-6


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TSSOP-16

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EDN contents

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Power this: testing audio ICs

42 SOCs for set-top boxes, television monitors, disk players, and mobile media players have or soon will have HD capability. But another aspect of this evolution—one that could prove even more challenging to SOC designers and test engineers—is that, along with HD video comes a significant increase in the quality of the accompanying audio.

by Ron Wilson, Executive Editor

Video-enabled home-networking technology trickles to market

37 Network bandwidth, latency, and signal disruptions limit deployment of distributed video by both consumer-electronics vendors and major service providers.

by Maury Wright, Editor in Chief

Comparing dc/dc converters' noise-related performance

55 Noise in dc/dc converters can differ from device to device. An understanding of the main dc/dc-converter topologies and their noise-performance disparities can help.

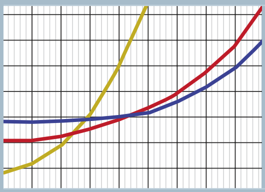
by Robert Marchetti, Vicor Corp

Optimizing handsets' multimedia connectivity and performance

61 Both consumer demand and competitive pressures are driving the rapid proliferation of handsets' multimedia capabilities. In striving to integrate the necessary peripherals, cell-phone architects and designers must make informed feature trade-offs when exploring architecture options.

by Rukmini Sivaraman
and Stephen Harris,
Cypress Semiconductor

DESIGNIDEAS



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Narrowband RF Transceiver

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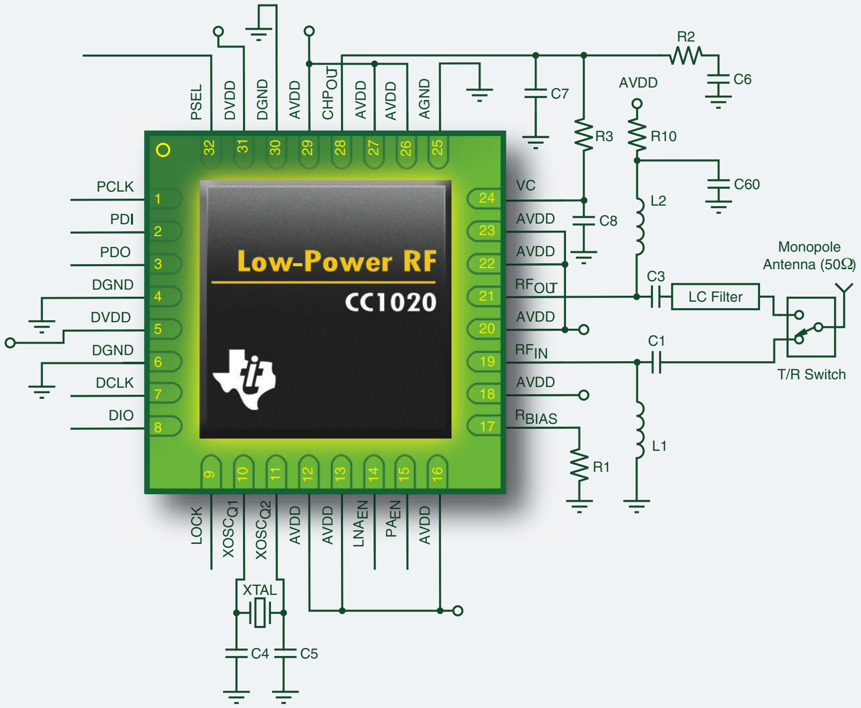

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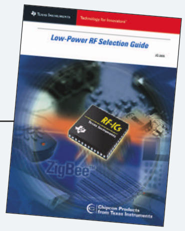
Chipcon Products from Texas Instruments

▶ Applications

- Narrowband applications in the 402 – 470 MHz and 804 – 940 MHz frequency range
- Wireless AMR
- Wireless alarm and security
- Low-power telemetry
- Remote keyless entry

▶ Features

- Channel spacing down to 12.5 kHz
- Blocking performance: 71 dB at ±2 MHz, 25 kHz channel spacing at 433/868 MHz
- High receiver sensitivity (up to –118 dBm for 12.5 kHz channel spacing)
- Low power consumption: 0.2 µA in power down, 19.9 mA in RX, 27.1 mA in TX at +10 dBm/433 MHz
- Programmable carrier sense indicator and digital RSSI output
- Programmable frequency in < 300 Hz steps
- CC1070 narrowband transmitter also available



Low-Power RF Selection Guide
Samples and Datasheets

www.ti.com/cc1020 ◦ 800.477.8924, ext. 2500

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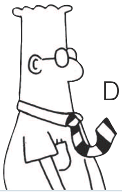

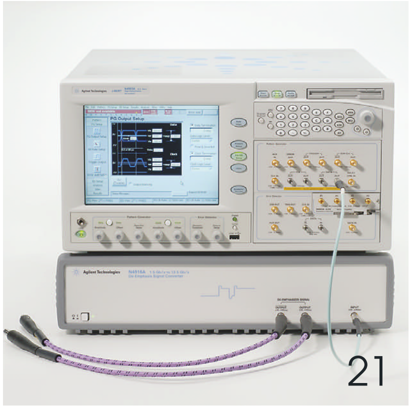

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DEPARTMENTS & COLUMNS

PRODUCT ROUNDUP

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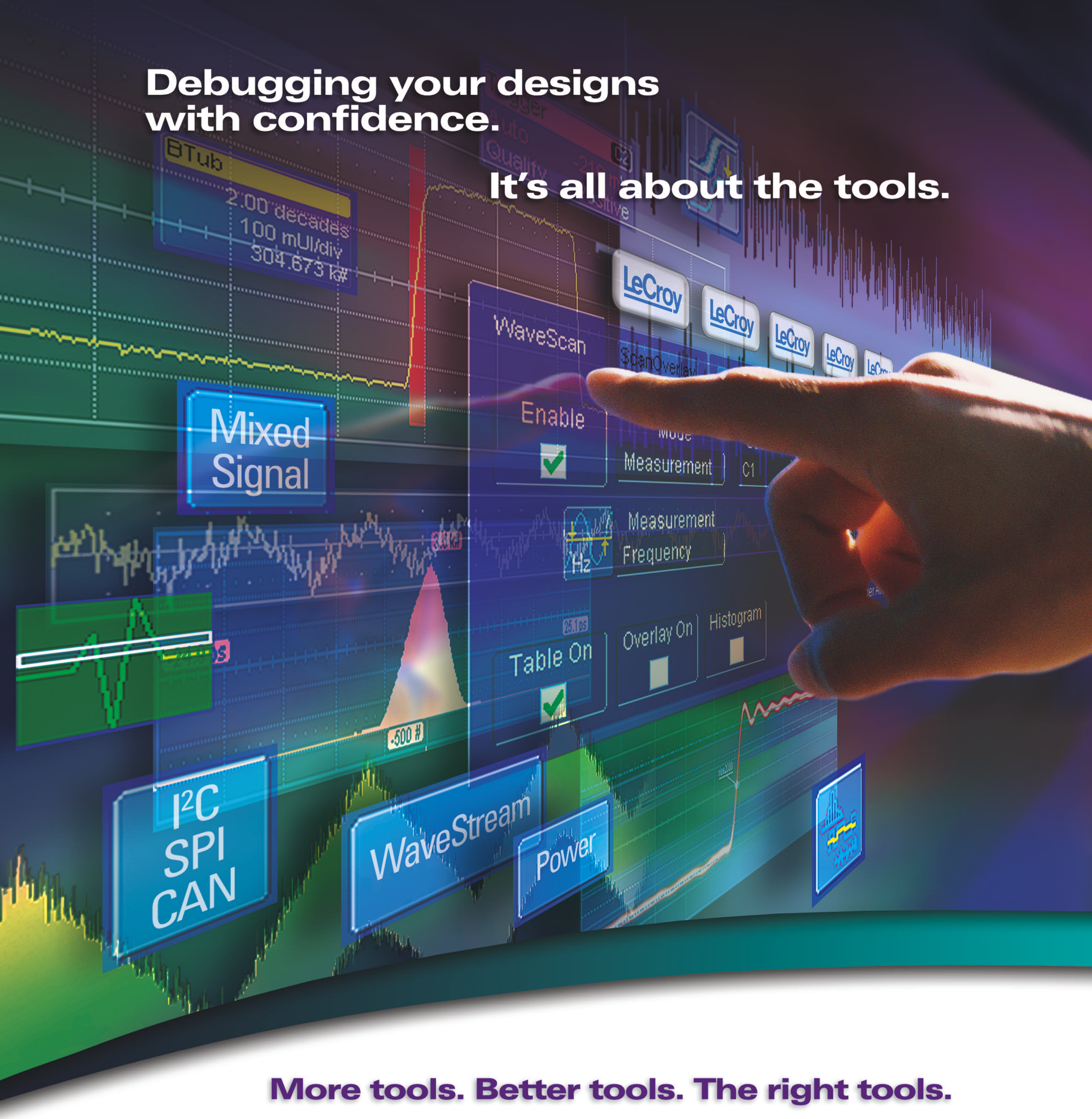

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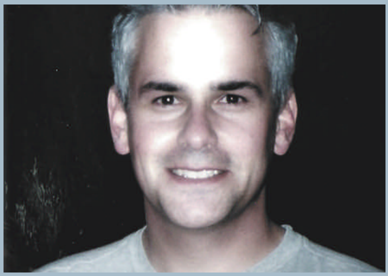

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Many designers spend way too much time, and thus their companies spend too much money, reverifying IP from vendors.
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The path to performance
Freescale makes a case for interchangeable 8- and 32-bit microcontrollers.
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Delving into display trends
Two years ahead of when ATSC will come to the forefront by virtue of the proposed NTSC shutoff date, is ATSC already obsolete?
➔www.edn.com/070301t1

Baby it's cold outside
Is your cell-phone battery pack smart enough to know it?
➔www.edn.com/070301t2

How long should a TV last?
It may have little to do with his EDA beat, but the above question posed by Senior Editor Mike Santarini touched off quite a conversation among disgruntled consumers.
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Miss this year's Demo show?
Editor in Chief Maury Wright, who sat through the whole thing, spotlights a few promising products and services, including inkless printing.
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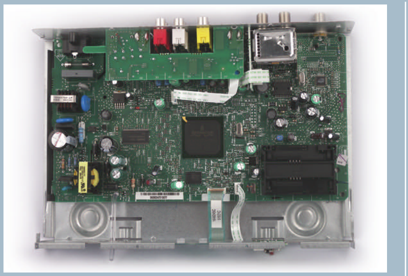

READERS' CHOICE

A selection of recent articles receiving high traffic on www.edn.com.

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Comparing DAC architectures
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Beyond Spice: Field-solver software steps in for modeling high-frequency, space-constrained circuits
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Model behavior: Creating embedded-software shortcuts
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Microcontroller drives logarithmic/linear dot/bar 20-LED display
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Optical feedback extends white LEDs' operating life
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The Hot 100 products of 2006
> www.edn.com/article/CA6399100

Soft-core processor gets an upgrade
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Using the HID class eases the job of writing USB device drivers
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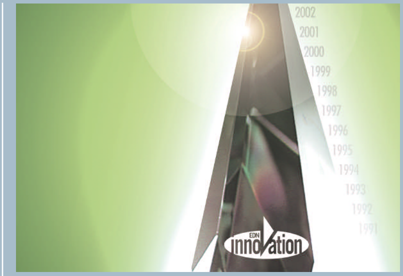

INNOVATION AWARDS

The votes are in. Now comes the fun part. Please join *EDN* April 2 in San Jose, CA, as we proudly present the 17th Annual Innovation Awards. Use the URL below to review the finalists, get event details, and buy your tickets.
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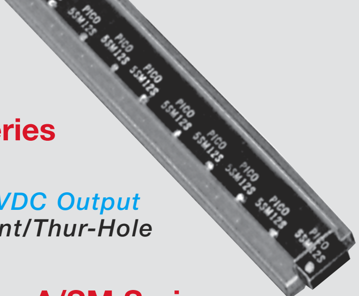

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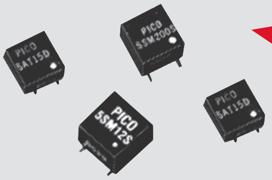

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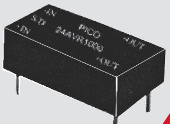

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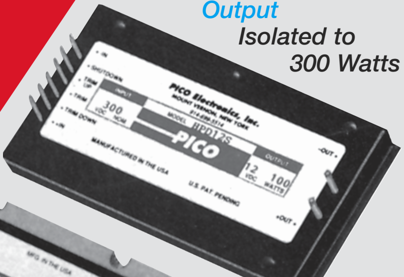

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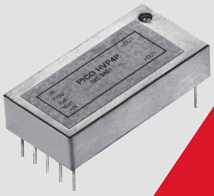

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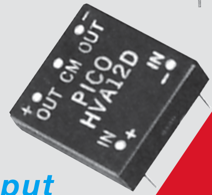

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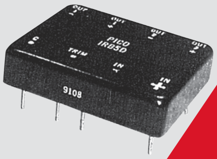

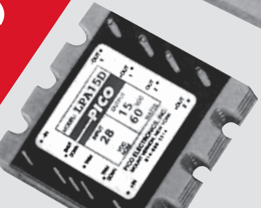

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BY MAURY WRIGHT, EDITOR IN CHIEF

Expert columnists cover analog, signal integrity, and chip design

In this issue of *EDN*, we're adding a new columnist to our stable of outside experts that bring you first-hand accounts of issues in the analog, chip-design, and signal-integrity areas. We welcome Pallab Chatterjee, who will be writing a column, "Tapeout," on chip-design and, occasionally, embedded-system-design issues. This issue also offers an appropriate opportunity to reintroduce you to our other expert columnists and tell you about some upcoming short instructional videos in signal integrity.

Chatterjee's first column, "The wheel goes 'round again," looks at how the chip-design industry is running through yet another evolutionary succession of similar steps in moving down to 65-nm and finer process geometries and to the world of SOCs (systems on chips). I believe that you will find Chatterjee an engaging addition to *EDN*. He has unimpeachable technical credentials with more than 20 years in the chip-design industry. He has for years operated his own consulting company and worked as a troubleshooter on chip designs at a who's who list of companies—both chip manufacturers and ASIC developers. He has hands-on experience with tools from all of the major EDA vendors. So, please enjoy "Tapeout," send me your thoughts on it, and send Chatterjee any topics that you'd like to see him cover in the future.

In addition to Chatterjee, our established-columnist roster includes Joshua Israelsohn, who covers the analog area in "Analog Domain"; Bonnie Baker, who covers analog and some system-design issues in "Baker's Best"; and Howard Johnson, PhD, who delivers his expertise in his "Signal Integrity" column.

Israelsohn spent a number of years as a full-time *EDN* editor between his current position with International Rectifier and his previous work designing analog chips at Analog Devices. Baker currently works in the data-converter group at Texas Instruments and also spent several years at Microchip. Baker also relatively recently published the book *A Baker's Dozen: Real Analog Solutions for Digital Designers*. Meanwhile, Johnson operates Signal Consulting. He presents both public seminars and private programs on signal integrity to engineers around the world. He has written a number of books, and he offers DVDs of what he calls Dr Johnson's SiLab (Signal Integrity Lab).

We've asked Johnson to share some useful tidbits from SiLab with you on our Web site. I hope that you will take the opportunity to tell me what you think of the short videos. By the time you read this editorial, the first five-minute presentation should be live at www.edn.com/techclips.

I'd also like to invite comments on all of our expert columnists. Each would love to hear from you about ideas for columns. I'd also like to hear about how we are doing with columns and about what other areas of the engineering world you think might warrant a columnist. **EDN**

Contact me at mgwright@edn.com.

INNOVATION BANQUET ON TAP FOR APRIL 2

As you know, we've been progressing though our annual *EDN* Innovation Awards program. Thanks to all of you that took time to vote. We're tallying the results as you read this.

I'd also like to remind you that tickets for the April 2 banquet in San Jose, CA, are on sale at www.edn.com/innovation. The festivities will include not only drinks, dinner, and a chance to see the brightest stars of the tech industry for 2006, but also the magic and comedy of Bill Herz. Don't miss it.

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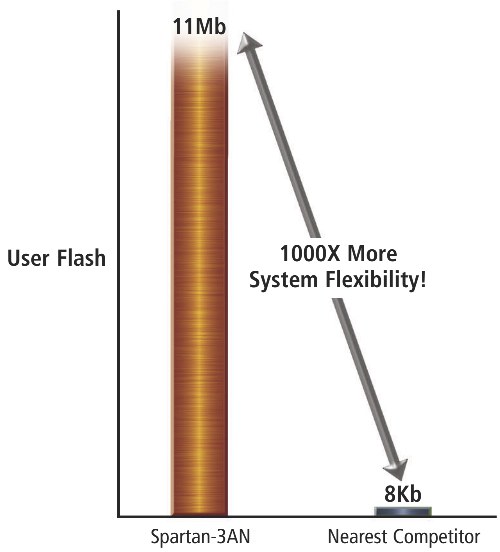

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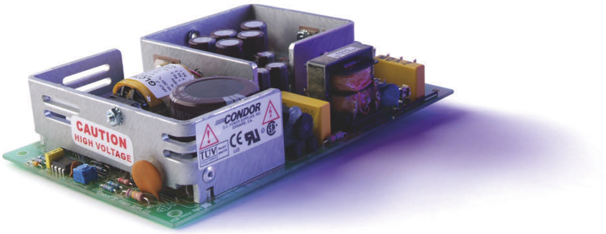

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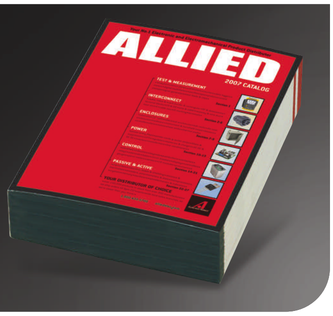

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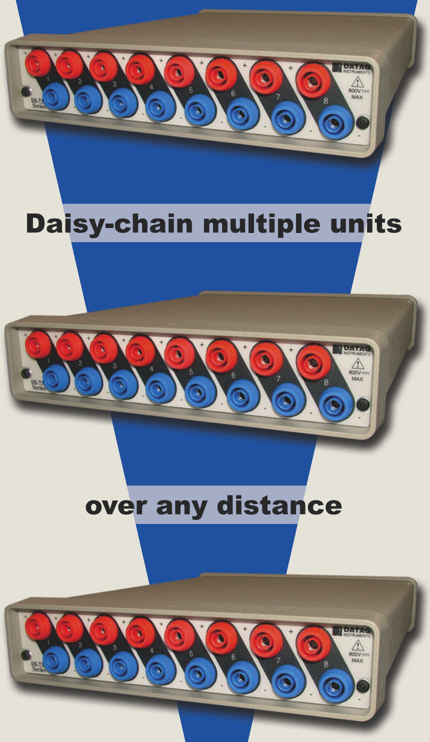

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INNOVATIONS & INNOVATORS

Don't blame the manufacturer for this product's confusing name

Agilent Technologies calls its latest signal generator—the N4916A—a de-emphasis signal converter because the standards body responsible for the technology that underlies the instrument refers to the technology as "de-emphasis," even though the common-sense name choice is "pre-emphasis." The instrument's key application is in characterizing receiver ICs for ultrahigh-speed serial buses, such as Generation 2 PCIe (PCI Express).

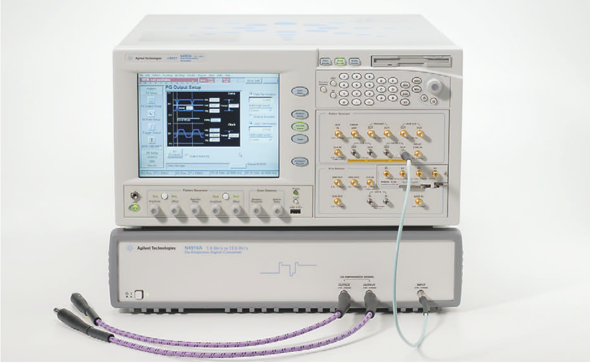
To use conventional, well-understood, and reasonably priced PCB (printed-circuit-board) materials, such as FR-4, at data rates higher than approximately 3 Gbps, you must compensate for the materials' high-frequency losses. These losses round the high-speed waveforms' normally sharp edges, causing received-data errors that manifest themselves as closures of what should be open eye diagrams. The cure is to pre-emphasize the transmitted waveform's leading and trailing edges—that is, to have the transmitter intentionally introduce overshoot, which disappears as the signal makes its way across the lossy board. The signal thus arrives at the receiver with rather-normal-looking edges.

The name confusion results from the valid circuit approach that introduces the overshoot: On pulses whose length exceeds a minimum value, the transmitter subtracts from the original signal an attenuated and slightly delayed version of itself, reducing the voltage during the waveform's flat portion. Someone must have decided that this reduction constitutes de-emphasis. It doesn't; the voltage reduction is an unintended minor consequence of the process's true purpose: pre-emphasis of the leading and trailing edges. Though it initially questioned the name, Agilent accepts it; the company has no interest in trying to change it.

When used as a front end for Agilent's J-BERT N4903A high-performance serial BERT (bit-error-ratio tester) and 81141/2A serial-pulse-pattern generator, the N4916A allows injection of signals with waveshapes suitably modified to analyze the channel effects under various de-emphasis and signal conditions. The unit also allows accurate characterization of receivers in a PCB environment, in which you need to inject de-emphasis to test the receiver's sensitivity and jitter tolerance under ideal and worst-case signal conditions.

The N4916A, which costs less than $40,000, offers the following benefits: accurate characterization and stress test by injection of a de-emphasized signal with variable postcursor in 0.5-dB steps; coverage of all popular and proprietary data rates to 13.5 Gbps; operation through the user interfaces of the Agilent J-BERT and serial-pulse-pattern generator; fast setup time with no manual adjustments; and worst-case device testing by injecting combinations of de-emphasis and jitter.**—by Dan Strassberg**

▷**Agilent Technologies**, www.agilent.com/find/N4916.



The N4916A de-emphasis signal converter, beneath the N4903A serial BERT, is a separate unit for use with several of the manufacturer's related instruments. Those instruments require no modification to work with the signal converter and to provide its user interface; hence, the converter becomes productive the moment you plug it in.

FEEDBACK LOOP

"The current mishmash of products and technology from various 'partnerships' is the key reason digital devices have not proliferated at a much faster pace."

—Steve Gates, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6406616. Add your comments.

LeCroy's cosimulator for serial-data-bus analyzers focuses on eye pattern

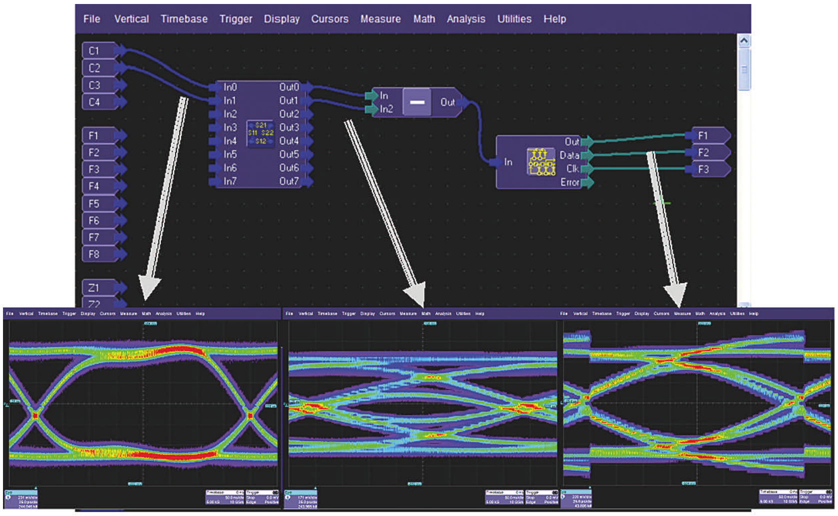
With serial buses operating at gigahertz speeds, designers of chips and boards that communicate with and over these buses often incorporate equalizers at the bus interface. Equalizers, essentially digital filters tuned for a particular bus's speed and loading, can introduce their own noise into the system, requiring specialized equipment to track a problem, deciphering whether the bus, the receiver, or the board is the culprit. Enter the serial-data analyzer, essentially a DSO (digital storage oscilloscope) just for high-speed-bus analysis and troubleshooting. These analyzers display data in the form of eye patterns. LeCroy has introduced the Eye Doctor, a cosimulation system for its serial-data analyzers that allows you to capture gigahertz signals, explore equalization schemes, capture and compare waveforms, and model output signals of simulated interconnects and transmission designs.

Eye Doctor includes Virtual Probing, which enhances the accuracy of measurements on distorted waveforms. Virtual Probing can simulate any signals within the system using a single measured waveform. Its Processing Web Editor connects the equalizer and the Virtual Probing elements in an intuitive signal-flow-diagram layout. You can use Virtual Probing to de-embed probe and fixture responses from measurements to improve the accuracy of signal-integrity measurements. Eye Doctor also incorporates equalized-receiver emulation, which simulates embedded waveforms as if you were able to probe: It reveals the signal as a real receiver would see it at the detector, a feature that probes lack. Equalized-receiver emulation includes FFE (feedforward equalization), DFE (decision-feedback equalization), clock recovery, and a variable-decision threshold.

The Eye Doctor is now standard on all newly shipped LeCroy SDA6000A, SDA6020, SDA9000, SDA11000, and SDA18000 models. It is also standard on the WaveExpert series SDA100G. Current SDA users can install Eye Doctor on their SDA units with a retrofit kit. The SDA family has a price range of $34,500 to $128,000.

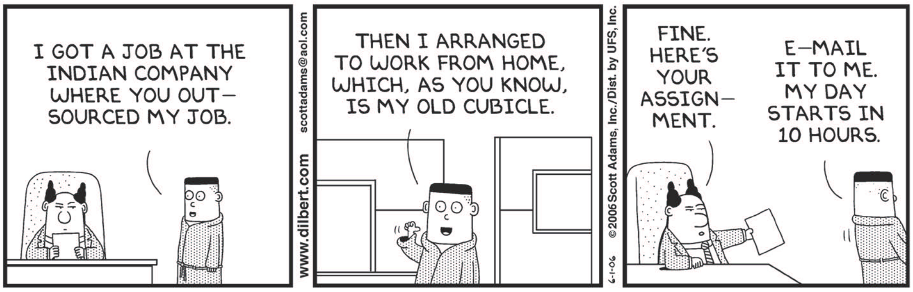
—by Margery Conner

▷**LeCroy Corp**, www.lecroy.com.



The Eye Doctor system uses Virtual Probing and equalized-receiver emulation to simulate signals through a serial-data-bus communication system, including embedded signals that you cannot probe at the receiver. The lower screens show (left to right) the measured signal at the transmitter, the virtually probed signal at the receiver, and the equalized signal.

DILBERT By Scott Adams



FEEDBACK LOOP

"We all know what the killer app is for PDAs, and that's making phone calls. Is Steve Jobs losing his magic? Absolutely not. I sat through the two-hour podcast of (his) keynote address, and the presentation, the concepts, and the new directions for Apple Inc. It was perfect."

—Jeff Pynnonen, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6406616. Add your comments.

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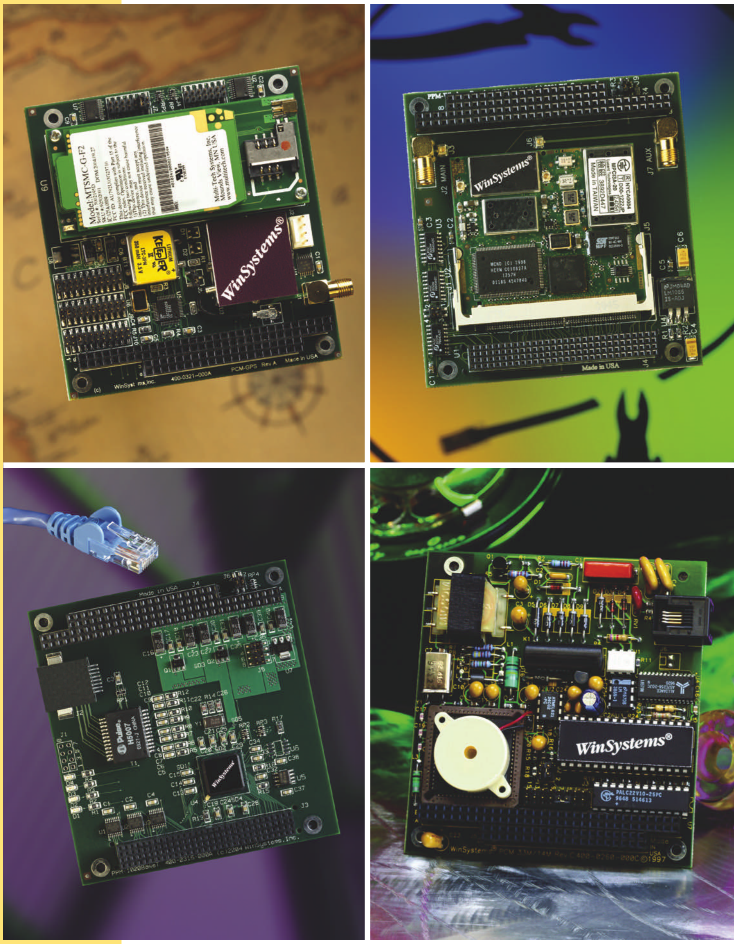

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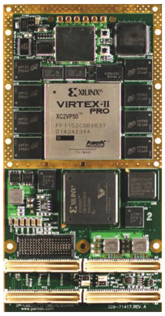
Software-radio transceiver fits harsh environments

Pentek's latest conduction-cooled, wideband software-radio transceiver targets harsh-environment applications, such as unmanned aerial vehicles and battlefield-communications systems. The Model 7141-703 PMC/XMC module features two 125-MHz ADCs and a Xilinx (www.xilinx.com) Virtex-II Pro FPGA (field-programmable gate array). Compatible with both CompactPCI and VME baseboards, the module has an extended-operating-temperature range of −40 to +70°C. Analog-input signals to the module are transformer-coupled to two 14-bit ADCs, and the digitized output signals go to the FPGA for signal processing. The FPGA also serves as a control and status engine with data and programming interfaces to each of the onboard resources.

Additional module resources include a quad digital downconverter; a digital upconverter with dual 16-bit, 500-MHz DACs; or a 512-Mbyte DDR SDRAM. Factory-installed FPGA functions include data multiplexing, channel selection, data packing, gating, triggering, and SDRAM control. The Model 7141-703 module complies with the VITA (VMEBUS International Trade Association) 42 XMC specification and supports high-speed, switched-fabric interconnects, such as Serial RapidIO and PCI Express.



The new Model 7141-703 PMC/XMC wideband software-radio transceiver features two 125-MHz, 14-bit ADCs and a user-programmable FPGA in a conduction-cooled form factor.

Pentek's GateFlow FPGA-design kit provides designers with all VHSIC VHDL (very-high-speed-integrated-circuit-hardware-description-language) source code and device configuration for the basic, factory-installed functions to allow users to add custom algorithms. The Model 7141-703 PMC/XMC device's prices start at $15,995, with delivery in eight to 10 weeks.

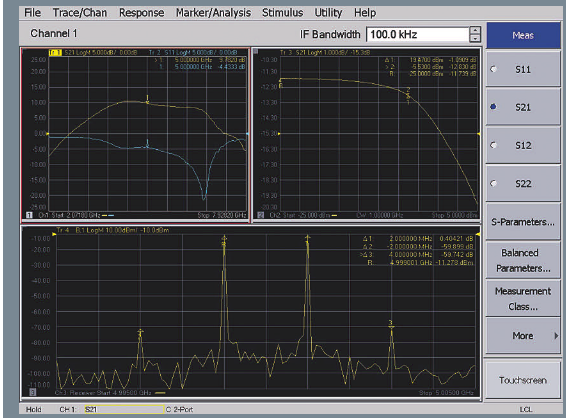
—by Warren Webb

▷**Pentek Inc**, www.pentek.com.

NETWORK ANALYZER'S SECOND SIGNAL SOURCE REDUCES TEST AND SETUP TIME, COMPLEXITY

Agilent Technologies has introduced the PNA-X network analyzer, which the company expects to become a new industry standard for microwave network analysis from 10 MHz to 26.5 GHz. The high-performance unit offers what the manufacturer asserts is a unique single-connection approach to two-tone and swept-local-oscillator measurements, featuring an integrated second signal source and signal-combining network. The highly integrated unit reduces test costs, setup time, measurement complexity, and the time required to make measurements on a broad range of components. The PNA-X targets testing of high-performance active devices, such as amplifiers, mixers, and converters, suiting it to the needs of development engineers in the aerospace/defense and wireless-communications industries.

Agilent based the configurable, two- or four-port, 26.5-GHz instrument on the PNA platform. According to a company spokesperson, the PNA-X is the only two-port network analyzer with an internal second signal source. A new signal-routing architecture transforms the unit from a pure network analyzer to an RF-measurement hub for amplifiers and frequency converters.



This PNA-X screen display shows both swept-frequency measurements (upper left and bottom) and a measurement versus a signal of varying amplitude (upper right).

The unit has two internal signal sources, each with 16-dBm output power, −59-dBc harmonics, a 40-dB power-sweep range, and a built-in pulse modulator and signal combiner. It easily measures amplifier-intermodulation distortion and makes traditional-S-parameter, pulsed-S-parameter, and hot-S22 measurements. It also measures harmonics and compression. You can use the integrated second signal source to produce fixed-IF or fast swept-local-oscillator signals for testing mixers and converters. The PNA's internal source lets you reduce test-setup complexity and realize speed improvements by as much as 35 times compared with traditional external sources.

Another key feature is an enhanced user interface. A large touchscreen, eight soft keys, and a simplified hard-key arrangement simplify operation without a mouse. These features also make it easier for engineers to quickly read multiple measurement results. The N5242A PNA-X network analyzer is available now at a starting price of $92,000.

—by Dan Strassberg

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Class G speaker amplifier includes charge pump

Maxim has recently introduced two monophonic audio amplifiers to drive speakers in mobile phones and other handheld systems. The MAX9730 drives conventional dynamic speakers; the MAX9788 works with new ceramic speakers. The parts provide 2.2W peak output and operate on 2.7 to 5.5V rails. They have 500-mA internal charge pumps that create negative supplies. This feature allows the bridge-tied output voltage to swing to twice the amplitude. The charge pump requires an external 4.7-µF capacitor.

Class G-output stages comprise conventional Class AB outputs with modulated supply voltages to reduce the voltage drop and hence power dissipation across the output transistors. Designers have traditionally implemented Class G-output stages using Class D stages to feed power to Class AB stages. The chips either enable or disable the internal charge pump to create two supply-rail levels. The AB-output stages in these parts have no efficiency advantage over any other AB-output stage except that they allow designers to choose speaker impedances. This feature thus allows designers to associate the maximum speaker volume with voltage swings fairly close to the battery-voltage-supply rails. This technique reduces power loss in the AB stage; however, you cannot employ this approach by itself because, as the battery voltage drops over the discharge cycle, the audio would start to clip as the battery-voltage-supply rails drop. At this point, these chips enable the internal charge pump and boost the output-stage supply voltage by lowering the negative rail from 0V to the negative supply of the battery voltage, ensuring efficiency and audio fidelity. PSRR (power-supply-rejection ratio) is almost −80 dB to 10 kHz, which ensures immunity from battery-voltage changes.

> “The combination of the internal charge pump and the bridge-tied output stage means that the MAX9788 can swing 14V p-p and thereby drive highly capacitive ceramic speakers.

The combination of the internal charge pump and the bridge-tied output stage means that the MAX9788 can swing 14V p-p and thereby drive highly capacitive ceramic speakers. These new speakers are far thinner than dynamic speakers and can allow mobile phones to be slimmer. The use of a charge-pump technology means that fewer EMI and RFI issues will occur.

The MAX9730 and MAX9788 come in 28-pin TQFN (thin-quad-flat-no-lead) packages, which dissipate 1.7W, and 20-bump micro-chip-scale packages, which dissipate 0.8W. The devices cost 73 cents (10,000).

—by Paul Rako

▷**Maxim Integrated Products**, www.maxim-ic.com.

The MAX9788 monophonic audio amplifier works with new ceramic speakers.

03.01.07

SOARING POWER COSTS PACE POWER-SUPPLY EFFICIENCY FOR SERVERS

A generation ago, aluminum producers located their smelters close to dams to take advantage of cheap hydroelectric power; now, server farms cozy up to dams for the same reason. Witness Google’s locating its newest facility in The Dalles, OR, on the banks of the Columbia River. Energy costs for datacom- and telecom-processing centers, where servers may number in the hundreds or even thousands, have skyrocketed: Energy costs outstrip equipment costs over the life of the server. In total, 59% of typical data-center power consumption is for power delivery, some of which goes to power-supply inefficiency and air-conditioning power to keep the supplies and servers cool. So, efficiency has become an important factor in selecting power supplies for servers. In addition, overall power density becomes important within server farms. Manufacturers want to cram as many servers as possible into their facilities, and, if the servers’ power supplies require massive power-sucking air conditioning, then the overall power density for the facility drops.

This reality is making digital-power supplies viable for servers. Previously, the additional costs of a processor and its attendant firmware development made digital control out of the question for the cutthroat pricing of “silver-box” (closed-frame)-enclosed supplies. With the reality of lifetime power costs making the additional digital-control expenses cost-effective, digital power is also becoming cost-effective because of its ability to react in real time to load fluctuations and to intelligently transmit operating information to the host.

With those factors in mind, power-supply start-up ColdWatt has introduced a digitally controlled family of ac/dc supplies ranging from 650 to 1200W that, the company claims, have efficiencies of 88 to 91% and can reduce power for cooling by more than 40%. The 1+1, 650W, redundant-configuration subsystem fits into a 1U rack, requires 4.3-in. width, and costs $143.51. The 1200W version provides N+1 redundancy with a 90.1% efficiency and power density of 15W/in.^{3} and costs $265.20.

—by Margery Conner

▶**ColdWatt,** www.coldwatt.com.

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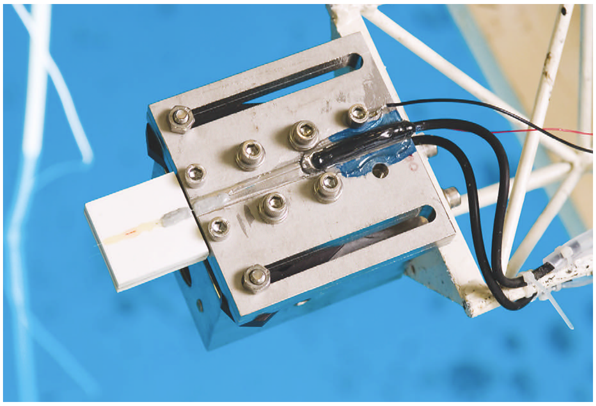


By mimicking principles of fish hearing, this underwater acoustic sensor provides better directional information than other available technologies.

RESEARCH UPDATE

BY MATTHEW MILLER

Underwater sensor hears like the fishes

A team at the Georgia Institute of Technology has developed an underwater acoustic sensor that improves upon earlier hydrophones by more accurately assessing the direction from which a sound emanates. Inspired by the inner-ear anatomy of fish, in which tiny hairs move in response to sound waves, the sensor features two plates attached by a hinge. One plate is fixed in position, and the other, which is made of a composite material that matches the density of water, is free to move. The movement of the second plate alters a signal in an optical fiber, which the researchers analyze using a photodetector.

Supported by a grant from the Office of Naval Research, the work may help the Navy reduce the length of the sensor arrays it tows around behind ships to accurately locate underwater objects, including submarines.

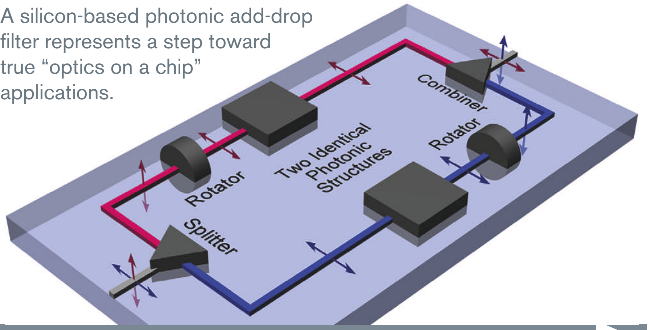
▷**Georgia Institute of Technology**, www.gatech.edu.

Photonic system has polarizing effect

Researchers at MIT have demonstrated the ability to accurately process arbitrarily polarized light in a densely packed photonic circuit. The breakthrough moves this essential function into the realm of compact, precise, cheaply manufactured silicon.

Microphotonic structures are sensitive to polarization, which has presented a problem because light waves moving through optical fiber can be either horizontally or vertically polarized. The MIT device achieves "polarization transparency" by splitting an incoming light beam into two polarized beams and then rotating the polarization of one beam before sending both through identical add-drop filters. Because the polarization matches, the filters respond identically to both inputs. As a final step, the circuit recombines the separate streams. Visit www.edn.com/070301ru1 for links to the original research and a peer-review analysis, both in the January issue of *Nature Photonics*.

▷**Massachusetts Institute of Technology**, www.mit.edu.



A silicon-based photonic add-drop filter represents a step toward true "optics on a chip" applications.

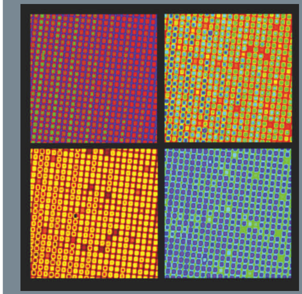
FREQUENCY COMB GETS UPGRADED TO BRUSH

Physicists at the NIST (National Institute of Standards and Technology) have created the first 2-D pictures of a frequency comb, enhancing the metrology tool's usefulness in applications such as optical atomic clocks, high-bandwidth communications, and remote sensing. The researchers developed a new method of separating and identifying thousands of frequencies of visible light to create a 2-D visualization that packs in far more information than a traditional 1-D comb image.

To make the images, the scientists fire a laser that emits about 1 billion pulses per second through glass filters and a metal grating that together direct each frequency of light in a specific direction. A digital camera then takes a picture of the resulting grid-shaped output, which the researchers liken to a brush whose bristles contain information about not only the frequency, but also the intensity of the light. For these images, the light passes through iodine vapor, revealing that substance's characteristic absorption pattern.

By enabling the measurement and manipulation of optical frequencies in a massively parallel manner, the frequency brush may help communications applications pack more channels into a given medium; play a role in optical-signal processing; and enhance sensing applications, such as trace-gas detection, according to NIST.

▶**National Institute of Standards and Technology,** www.nist.gov.



Researchers have added another dimension to the frequency comb, resulting in a "frequency brush" that may enable advances in communications and remote sensing.

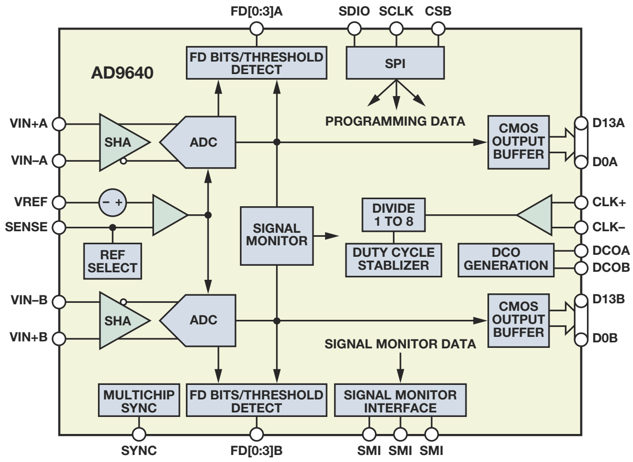
LEADING inside

A series of engineering insights
by Analog Devices.

Data Converter Function Can Help Solve Cost and Size Design Challenges in 3G and 4G Wireless Infrastructure

As usage and demand for competitive services continue to rise, manufacturers of wireless infrastructure, especially 3G and 4G, must constantly reduce the size and cost of newly installed wireless infrastructure, while holding to high standards of performance, functionality, and quality of service. The data conversion block is a critical function in wireless infrastructure designs, and selecting a converter that is targeted for this application is key to improving the overall system design and breaking through design barriers such as size and cost.

14-bit, 150 MSPS ADC in 9 mm × 9 mm 64-lead LFCSP targets wireless infrastructure



In the main receiver function, the analog-to-digital converter (ADC) is the key block that digitizes the incoming intermediate frequency (IF) signal (after it has been mixed down from the antenna) and then passes the digital data to the digital downconverter. Most architectures require two receivers, called main and diversity, each requiring a high performance, high speed ADC. Until now, sampling rates beyond 135 MSPS could only be realized by utilizing single-channel 14-bit ADCs. This constraint necessitated implementing two separate converter blocks, with their associated requirements in power, PCB area, and cost. The new ADC solution from Analog Devices, the AD9640, dual, 14-bit, 150 MSPS A/D converter, addresses this issue. This dual device enables a 50% reduction in converter board space requirements in the main and diversity architecture. And the AD9640 contains additional attributes that improve wireless infrastructure system design.

A 150 MSPS ADC sampling rate simplifies some of the signal chain complexity and cost associated with a communications design. As sampling rates increase, analog input filtering requirements decrease, and the reduced filtering complexity results in lower cost. Also, because the AD9640 can sample an IF input signal as high as 450 MHz, an analog mix down stage can be eliminated from the receiver input signal chain. This attribute functionality allows savings in board space and cost, and improves performance through the elimination of an analog block and its associated noise contribution.

The power reduction in the AD9640, vs. the previous single ADC solutions, provides benefits for base station design. Because many new wireless infrastructure systems are being mounted on outside poles, they cannot utilize active heating and cooling systems as afforded by equipment sheds and buildings. By consuming a relatively low 390 mW/channel, the AD9640 simplifies the mechanical and passive thermal design requirements of the pole-mounted transceiver enclosure.

The high performance level achieved by this dual ADC also contributes to significant cost savings in a wireless infrastructure design. Within the radio receiver there is an automatic gain control (AGC) loop that controls the strength of the desired incoming signal. The function of the AGC is to maintain a fixed input signal level to the ADC to ensure that it meets the dynamic range requirements of the system. As a cell phone user moves farther away from the cell tower, the AGC loop increases its gain to ensure adequate reception. If the ADC has a higher signal-to-noise ratio (SNR), the AGC loop does not need as much gain because the ADC can resolve smaller signals and can operate with reduced input levels. Likewise, large interfering signals can cause the ADC to generate spurious components or harmonics. ADCs with higher SFDR performance allow the system to tolerate larger interferers without having to adjust the AGC. In both cases the AGC circuit can be simplified or eliminated with a high performance ADC like the AD9640, which delivers SNR of 72.7 dBFS, and an SFDR of 85 dBc, with a 70 MHz IF input.

Analog Devices offers a wide portfolio of ADCs for communications applications. For data sheets and additional information on the AD9640, visit *www.analog.com/AD9640* or call 1-800-AnalogD. ▶

*Author Profile: **Chris Cloninger** is the business development manager for Analog Devices' High Speed Signal Processing Product Line.*

BY HOWARD JOHNSON, PhD

OFC madness

Ernie, a sometime correspondent, writes: The power cord on my oscilloscope broke because we stepped on it too many times. I heard that OFC cryogenic power cables are really good but expensive (hundreds of dollars). Should I replace my cord with one of those?

Howard: In this context, OFC stands for oxygen-free copper. Such copper must smelt in a special oxygen-free atmosphere to reduce the amount of oxygen latent within the copper. Sound expensive? It is. Physicists use the stuff inside vacuum chambers to reduce oxygen outgassing.

The term "cryogenic" implies that the conductors making up the power cable have been cryogenically cooled, probably in liquid nitrogen. That process can in some cases produce large, uniform crystalline grains within the body of the conductor.

What kind of exotic, high-tech application could possibly justify the use of such elaborate techniques for its ac power cable? Several suppliers would have you believe it is something you already own—your audio amplifier.

Ernie: You are right; it does seem to be an audio thing. I checked out some audiophile reviews on the Web, and they say that OFC cryogenic power cables can "restore the texture, dimension, and spatial cues in sound and video that EMI and RFI often obscure" and provide "deeper, blacker backgrounds and a richer tonal balance."

Howard: Let's look at the facts, not the fantasy.

Ordinary 60-Hz power travels miles from the nearest power station over ordinary, oxygen-rich, noncryogenically frozen wires laden with bird poop. It goes through a local distribution transformer (gobs more regular wire in there) and then travels hundreds of feet more through your house wiring to a local outlet. Do you think the last 6 ft of cryogenically altered, helically wound, hand-braided, eight-gauge wire makes any sensible difference?

> What do you really need in a power cable? Insulation is a good idea. Stranding is good, too.

You could probably solder together old, rusty coat hangers and do just as well, provided you don't have any young children or pets in the house.

So what do you really need in a power cable? Insulation is a good idea. Stranding is good, too. Stranded wire is flexible enough to bend many times without breaking. That's all the technology you need.

Ernie: How about shielding? A lot of high-end audio-power cables are shielded.

Howard: It's a nice idea, but because all the other wires in the house lurking behind the dry wall remain unshielded, it doesn't help to shield the last little 6-ft chunk.

Ernie: OK, how about silver plating? The best power cords have to be silver-plated, don't they?

Howard: Silver plating minutely reduces skin-effect losses at high frequencies. Some RF applications use it. It has no measurable effect on small power cables at 60 Hz.

Ernie: What about EMI-noise rejection?

Howard: Your equipment, if it is worth its salt, already has a built-in power-line noise filter.

Ernie: I've heard that a good power cord aligns the flow of electrons into your equipment for maximum performance.

Howard: What? That whole idea is bonkers. The mean free path for electrons in copper is about 0.039 microns. Electrons are constantly slamming into something and changing direction. There is no "aligned flow." Only superconductors can do that. The only super thing about an OFC power cable is the profit margin.

For your application, just get a heavy-duty cable with a thick jacket, and put a rubber floor mat over it. EDN

MORE AT EDN.COM

Go to www.edn.com/070301hj and click on Feedback Loop to post a comment on this column.

Howard Johnson, PhD, of Signal Consulting, frequently conducts technical workshops for digital engineers at Oxford University and other sites worldwide. Visit his Web site at www.sigcon.com or e-mail him at howie03@sigcon.com.

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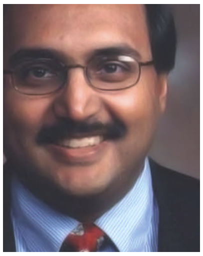

BY PALLAB CHATTERJEE, CONTRIBUTING TECHNICAL EDITOR

The wheel goes ’round again

Recent technology and product announcements remind me of the saying, “Everything old is new again.” This phrase has been popping into mind more frequently as industry pundits herald new bottlenecks and incremental solutions to process- and design-tool issues as revolutionary. For design and EDA veterans, again hearing these discussions jogs the memory a bit.

Leading issues in design-verification tools have changed from those involving specialized hardware platforms with software, to hardware emulation, to just software tools on stand-alone stations. The first generation of EDA comprised hardware-and-software vendors, such as Daisy Systems and Mentor, which were promoting optimized hardware platforms to effectively use their software. Today’s designs run on general-purpose hardware, but, due to data size, specialized hardware is still sometimes necessary to meet schedules. The most recent entries in this area are Brion’s OPC/PSM (optical-proximity-correction/phase-shift-masking) products and Mentor’s Calibre nmOPC product, which can now support hyperclusters of multicore-cell processors. As with the past models, hardware and information-technology costs can exceed the costs of the software running on them.

The advent of 45-nm processes returning to metal-gate CMOS; the industry’s embrace of immersion lithography; the emergence of machine-specific, model-based OPC; and the use of topology- and orientation-based design rules are reminiscent of the greater-than-10-micron, metal-gate-MOS days. Those were the days of machine-specific contact-printing rules; serif and notch insertion for critical-layer imaging; and pre-EPI (epitaxial-silicon), pre-implant (spun on dopants) wafer processing. Breakthroughs stabilized these flows, and, given time, the same should result for 65-nm and smaller processes.

Process modeling and characterization are also undergoing a spin of the wheel. Due to the costs of running and testing the cells, engineering is shifting from kit parts or silicon-proven macrocells, primitive cells, and blocks to simulation-verified designs. This scenario results in a perception that the entire process window can’t adequately cover multiple views of the design, including timing, power, noise, ac performance, and leakage. The reality is that most designers have long dealt with the uncertainty of device and macro models, and they have always had to deal with nonstandard views as part of a specification. The short time during which the abstracted models and reduced view analysis were sufficient to complete a design was the exception, not the rule. Thus, the industry is not facing a new design crisis; it’s just returning all design engineers to the same task list.

Another crisis the industry’s waving around is on-wafer variation. This is the same issue that existed in the transitional days of 2-in. metal-gate wafers to exotic, 4-in. silicon-gate wafers and at the start of widespread use of EPI on the wafers. Equipment manufacturers spent a lot of time and money on research and development to address these issues, and, with the chip-design groups, they found solutions, so that they have been nonissues for more than 20 years. There is no reason to believe *this* issue is unsolvable.

On the design-verification side, the proliferation of SOCs (systems on chips), with their limited access to internalized signals compared with partitioned systems, has started to shift. This shift is moving from Stage 2, hardware emulation, to Stage 3, a pure software base, with the current generation of hardware/software co-verification, mixed-mode-simulation, and ESL (electronic-system-level) tools. The last big breakthrough in this area was the widespread adoption of scan and BIST (built-in self-test) to improve verification coverage. I am not sure whether ESL is strong enough to completely turn the wheel to its next stop, but it is certainly causing some movement. The industry is still debating the direction of this movement.

Engineers solved everything in the past through a combination of good engineering and perseverance, and they will do so again. Design and manufacturing groups should continue their course of innovation and development through collaborative research and development. And the EDA community should stop declaring every little problem a crisis and every minor product release a revolutionary development. EDA is just one aspect of the engineering chain; it’s not the driver for all technology. As soon as the equal collaboration of design, manufacturing, EDA, and IT/communications comes together, we can get on with discussing the impact of product innovation and its benefit to a global society.EDN

Contact me at pallabc@siliconmap.net.

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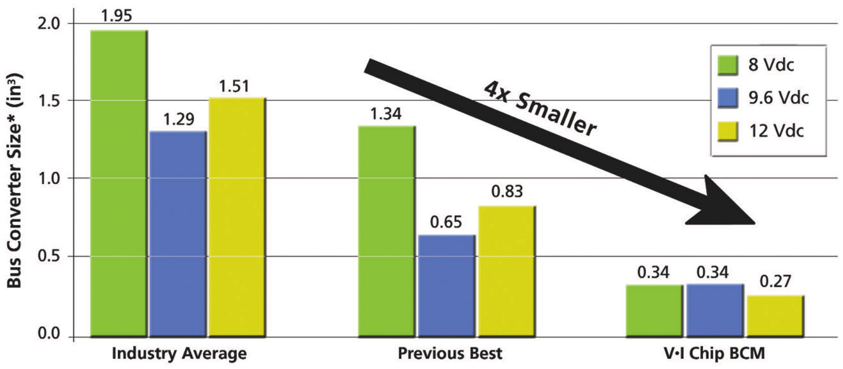

* Bus Converter package size normalized for 300 W output

48 Volt BCM Range

BCM Model No.	Vout (V)	Max Power (W)	Peak Efficiency (%)
B048F015T14	1.5	140 W	91.5
B048F030T21	3.0	210 W	95.0
B048F040T20	4.0	200 W	94.8
B048F060T24	6.0	240 W	95.6
B048F080T24	8.0	240 W	96.0
B048F096T24	9.6	240 W	96.2
B048F120T30	12.0	300 W	95.1
B048F160T24	16.0	240 W	96.0
B048F240T30	24.0	300 W	95.7
B048F320T30	32.0	300 W	96.5
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BY GLEN CHENIER • TEETER TOTTER TREE STUFF

EMI woes and cures

DANIEL VASCONCELLOS

Ever since the first poorly shielded home computers caused annoying herringbone patterns or worse on neighbors' television screens, the FCC (Federal Communications Commission) and other agencies worldwide have mandated strict limits to the levels of RF emissions that a digital-logic product can spew into the environment. The usual measurement practice for a new product release is to set up the equipment under test in a large, shielded, anechoic chamber to identify all radiated frequencies greater than 30 MHz and then move the equipment to an open area outdoors for the actual amplitude measurements of each of these frequencies. Many first attempts result in dismal failures.

Once a designer's equipment fails the test, he has to figure out how to fix the problem. Yeah, right. Test of any trial fixes requires an expensive and time-consuming trip to the test site, unless the designers have access to an in-house measurement facility. In most cases, they don't: Anyone who has ever tried to measure the emissions from a single product in a digital-electronics lab that many design teams and their operating hardware share quickly realizes how useless and impossible this attempt is.

My first exposure to EMI (electromagnetic-interference) measurement was in trying to make my multiport, unshielded-twisted-pair Ethernet-hub card comply with FCC Part 15 Class A in a multicard chassis that leaked RF like a sieve. The mechanical designers would not believe that faceplate grounding contacts made from coiled springs were useless at radio frequencies and deemed low-inductance beryllium-copper fingers "too expensive" to use. Management told the hardware engineers to make their boards quieter instead. We did not have a screened room, but we did have a spectrum analyzer and a leftover, front-end, wideband-RF amplifier.

All the other designers' cards for this product failed at the open-area-emissions test site. When my turn came, my card was 20 dB over the limit at the worst frequency of 80 MHz. I had the site technician make a swept plot of the emissions starting from 0 instead of 30 MHz. (The reason? It makes for a paper plot that you can easily interpret later to find the offending frequencies.)

I then went back to the lab, grabbed the spectrum analyzer, sneaked my test setup into the basement, and hung an 80-MHz dipole antenna from the ceiling. Lacking a screened room on the premises, I found that a basement is the next best thing for removing most ambient RF from radiated measurements. I hoped to find ways to reduce the emissions at the board level.

I had three days of RF-emissions-mitigation practice before my colleagues discovered me and moved their test setups down into the basement, too. The presence of their added equipment required me to recalibrate the correction factors between the basement and the open-area site for each radiated frequency. I was not interested in absolute levels, room reflections, or antenna-correction factor; I cared only about how much I could reduce the offending frequencies without raising other frequencies beyond their limits, which I again derived from the differences in their basement-versus-open-area plotted levels. The open-area site gave me the required reduction at each frequency in the plot; I had only to reduce the basement levels by the same amount. Specifically, I had to reduce the 80-MHz emission by 26 dB. This requirement took a lot of explaining to those who could not understand the concept and kept insisting that basement measurements were meaningless.

I did a board re-spin and headed back to the open-area test site. This time, my card passed with a 6-dB margin at the worst frequency of 80 MHz, and we could ship it. Yeehaw! **EDN**

A former telecom engineer, Glen Chenier is now a design consultant for a fail-safe-server-power system. Reach him at glen@teetertottertreestuff.com.

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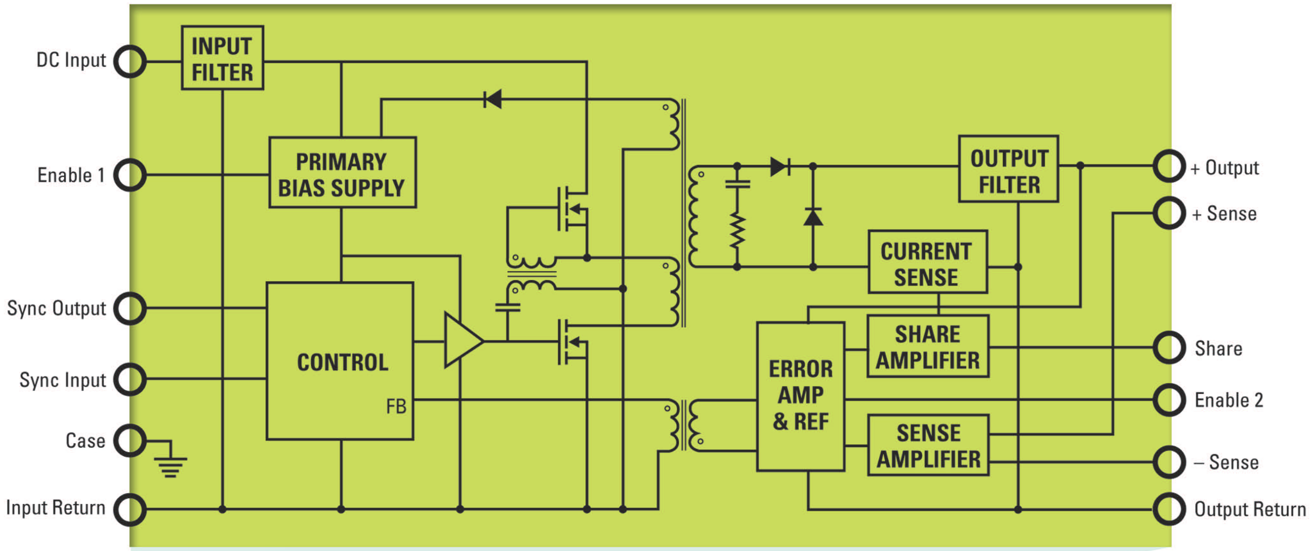

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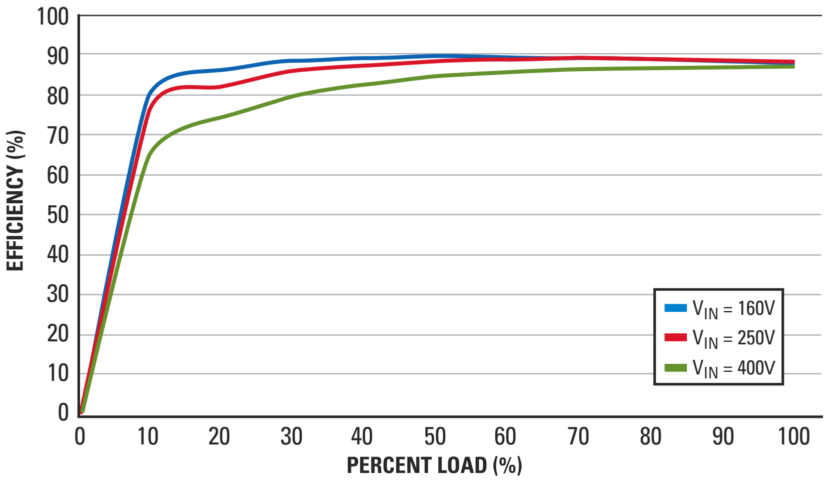

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NETWORK BANDWIDTH, LATENCY, AND SIGNAL DISRUPTIONS LIMIT DEPLOYMENT OF DISTRIBUTED VIDEO BY BOTH CONSUMER-ELECTRONICS VENDORS AND MAJOR SERVICE PROVIDERS.

Video-enabled home-networking technology TRICKLES TO MARKET

BY MAURY WRIGHT • EDITOR IN CHIEF

Consumers have readily adopted home networks to share Internet connections, files, and printers. And, although some consumers have wired networks that use the same Category 5 cable that businesses use, more consumers rely on "no-new-wires" technologies, such as HomePlug power-line networks or Wi-Fi (IEEE 802.11) wireless LANs because these choices don't incur costly cable installation. Now, with the transition to digital representations of music and video virtually complete, we need to move multimedia-data streams over home digital networks, as well. Note that the "we" is purposely ambiguous, because consumers want their entertainment throughout the home, and consumer-electronics vendors and service providers want to offer the same thing. But, thus far, the no-new-wires options struggle to distribute video in real time.

If there is a single device that has prompted the demand for video-capable networks, it's the DVR. Consumers have enthusiastically adopted TiVo and DVRs from cable or satellite companies because of the simplicity of recording programs and the ability to pause live programming and fast-forward through commercials. And consumers would now like to replicate that experience. Nick Chakalos, senior director of software-product management for the Motorola Connected Home group, says, "When they sit in front of the second, third, or fourth TV, they want that same experience."

To some extent, a DVR connected to each TV would solve the consumer demand. Indeed, satellite- and digital-cable-TV providers have conditioned consumers to accept an STB (set-top box) that controls each TV. But the DVR is more problematic. Putting a disk drive into each STB still means that the program of interest might not be on the STB of choice at any given time unless you in some way link the STBs. A better answer is networked STBs than can share programs stored on one disk drive.

Competing TV services from the legacy telephone carriers will increasingly demand video-capable networks, as well. The telephone carriers, such as AT&T and Verizon, are pushing to offer video over IP (Internet Protocol) using either DSL (digital subscriber line) or fiber to the home (**Reference 1**). Generally, the term "IPTV" (Internet Protocol TV) implies an architecture in which an STB receives a video stream over IP and decodes and displays that video. The STB sends channel changes at the STB up the network to carrier equipment. So, an IPTV deployment to serve three TVs in a home will require three networked STBs, and the network will need the bandwidth to carry the three video streams in addition to Internet traffic.

HDTV (high-definition TV) adds to the demands on home networks because higher resolution implies a faster data stream to serve the video. Whether the application is a shared DVR, IPTV, or both, each HDTV stream can require a

AT A GLANCE

- No-new-wires technologies haven't hurdled the video obstacle.
- Carriers may need a mix of technologies for different applications and regions.
- The 802.11n standard has perhaps the most promise, but standards skirmishes continue to burden it.

Figure 2 A multisegment smart antenna allows Ruckus Wireless' 802.11-based MediaFlex products to deliver video over long range and with no signal fading.

continuous 10-Mbps or faster stream on the home network. And note that the video application requires data delivery in real time. The STBs at each TV will not buffer more than a few seconds of the streaming program in the decoding process. Any significant latency in stream delivery interrupts the program that the STB delivers to a TV.

Consumers using home networks don't notice problems that would be deal killers for video. For example, signal fading can cause Wi-Fi networks to retransmit packets. For the Internet surfer, the result is a slightly slower page download. Dropped packets can mean a program interruption to video. So, home-video networks will need a combination of the aggregate bandwidth needed to deliver multiple video streams and QOS (quality-of-service) provisions that minimize disruptions in packet flow.

Proponents of the various home-networking technologies have been vigorously preparing for video delivery, believing that the first to handle video well would become the long-term winner in the home. The efforts have included the development of faster data rates and QOS network layers.

The list of candidates starts with Category 5 cable. Increasingly, new homes have this cable, just as offices do. In other cases, service providers or home owners have retrofitted homes with Category 5. The no-new-wires approaches either rely on wireless or attempt to use power-line, phone-line, or coaxial wiring that's present in most homes. In the wireless camp, some flavor of 802.11 or Wi-Fi is the likely choice, although some in the UWB (ultrawideband) camp also hope to play in the market. The HPNA, or HomePNA (Home Phoneline Networking Alliance), group is the driver of phone-line technology.

Several companies and industry groups have targeted the coax-cable plants that are present mostly in North American homes. For instance, even the HPNA group now claims its technology works over coax as well as phone lines. Coaxsys has also developed coax-capable products. But the MOCA (Multimedia over Coax Alliance) group that Entropic Communications originally spurred seems to have the most momentum in the coax area. In the power-line area, both the Intellon-driven HomePlug

Figure 1 The Follow Me TV technology from Motorola will yield a distributed network of set-top boxes that allows consumers to view any live or stored programming anywhere in the home.

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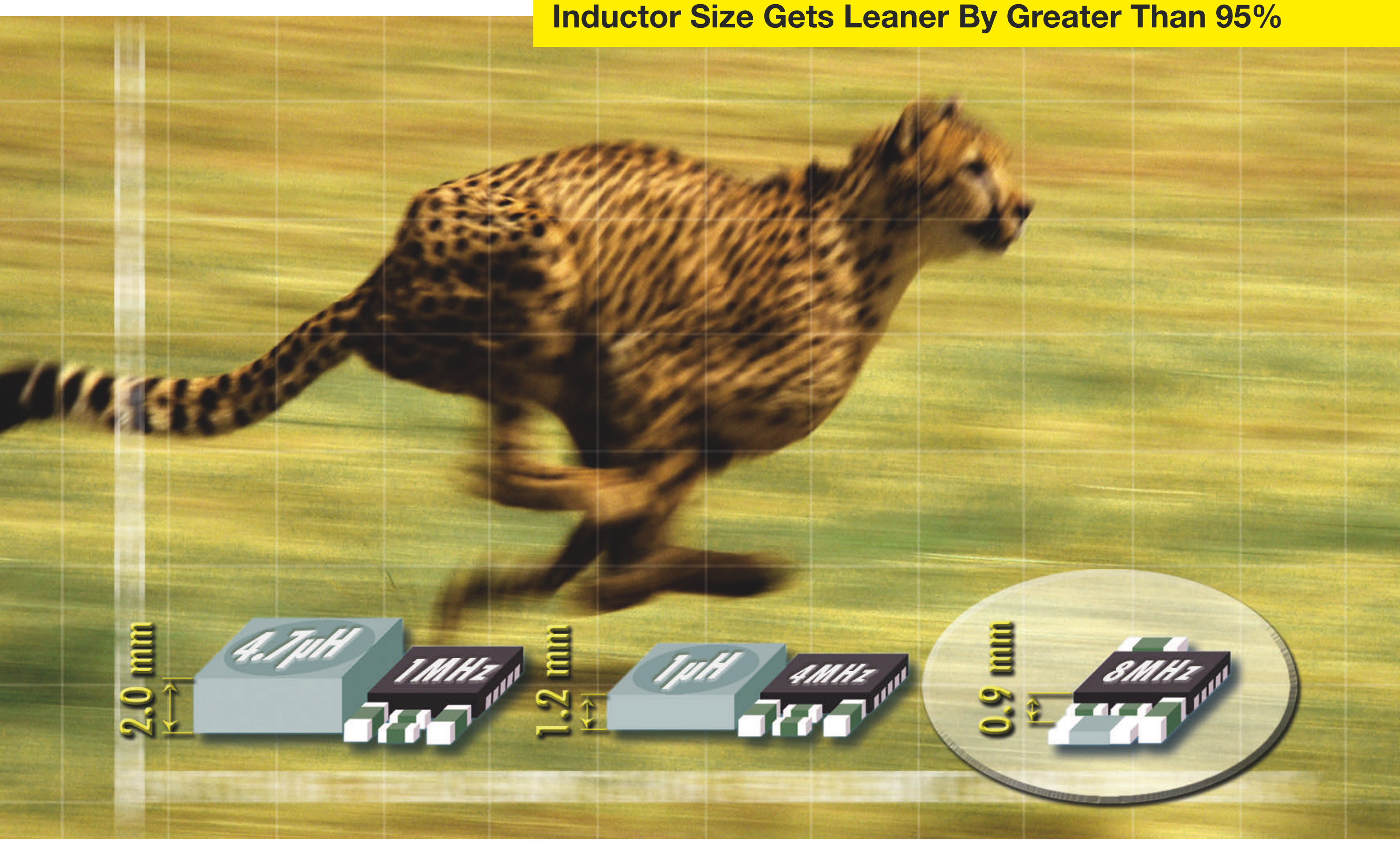

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⊞ **Check out the Web version of this article at www.edn.com/070301df for more details on various no-new-wires technologies, including a sidebar on in-room wireless video and a vendor box. Come back throughout the year for updates as products ship with embedded-video-network technologies.**

When *EDN* scheduled this article, we expected the Consumer Electronics Show in January to yield real consumer products or products to be deployed by service providers that embedded technology from most of the aforementioned candidates. Although all performed videocentric demonstrations, little in the way of deployment is happening. Still, we expect near-term activity. So, at the Web version of this article at www.edn.com/070301df, we'll provide a current status of each candidate and updates that detail any real products as the year passes.

For now, however, let's focus on what *is* happening, and it's compelling. Motorola has been the most aggressive among the STB players in pushing a distributed-video architecture. The company based its Follow Me TV service on the notion of getting the full DVR experience anywhere in the home (**Figure 1**). Verizon, in its FIOS (fiber-optic-services) deployment, is shipping Motorola STBs with the Follow Me technology.

The Verizon deployment is a relatively simple replication of DVR functions on each STB, with a hard drive present only in the main STB. But Motorola has more in mind. Motorola's Chakalos claims that the technology will ultimately virtualize the tuning capability and storage resources in a home. He describes a scenario in which one STB includes dual tuners and a hard drive, and two remote STBs include single tuners. Motorola intends for the consumer to see that distributed system as a four-tuner DVR accessible from anywhere in the home. Likewise, consumers would see one storage resource for the entire house, even if the entire library relied on hard disks in multiple DVRs and even music or photo libraries from home PCs. Motorola hopes to begin rolling out this more advanced technology this year in a Comcast-cable deployment.

For now, Motorola is relying on MOCA to deploy Follow Me STBs. Chakalos claims that MOCA can today support the goal of three- to four-TV homes with HDTV support. But Chakalos is quick to say that Motorola is also testing and even investing in the other no-new-wires technologies. MOCA has a number of wins in other regions of the world, as well.

On the Wi-Fi side, the industry has great hope that 802.11n will finally make video distribution possible, especially when bolstered by the 802.11e QOS layer. But the industry has continued to battle over the 802.11n standards process. The industry expects a final standard to emerge this year, and "draft-compliant" products are already rolling into the home-data-networking market.

But Ruckus Wireless is the only company that's made real headway into Wi-Fi-video delivery. Ruckus doesn't actually make 802.11 baseband technology. Instead, the company has developed the BeamFlex smart-antenna scheme, which relies on a multisegment antenna and which extends range and eliminates signal fading. (**Reference 2** provides some detailed hands-on tests that *EDN* performed on early Ruckus products.)

Ruckus Director of Marketing David Callisch claims that the company has delivered 100,000 of its MediaFlex systems, which comprise an access-point and client-device pair, to consumers through service providers in the IPTV market (**Figure 2**). The success has come largely in IPTV deployments by small regional carriers in North America, Europe, and Asia. The product relies on Atheros Wi-Fi ICs.

What can we expect for the rest of 2007? AT&T is committed to using HPNA technology in its U-Verse IPTV service. But that deployment is still in an early stage. Callisch claims that Ruckus has a prototype 802.11n product that can handle three HDTV streams. But he doesn't expect carriers or consumer-electronics companies to adopt 802.11n in 2007 because of the delay in finalization of the standard and the confusion of the draft-compliant products from chip vendors.

It's increasingly looking as though all of the home networking candidates might get a piece of the market. In fact, Motorola's Chakalos says, "We would like to see them all happen." Chakalos, for instance, believes that 802.11n will prove useful in video distribution in North America but that brick-and-concrete construction in many European homes may limit the use of wireless in video distribution.**EDN**

REFERENCES

For the two references associated with this story, visit www.edn.com/070301df.

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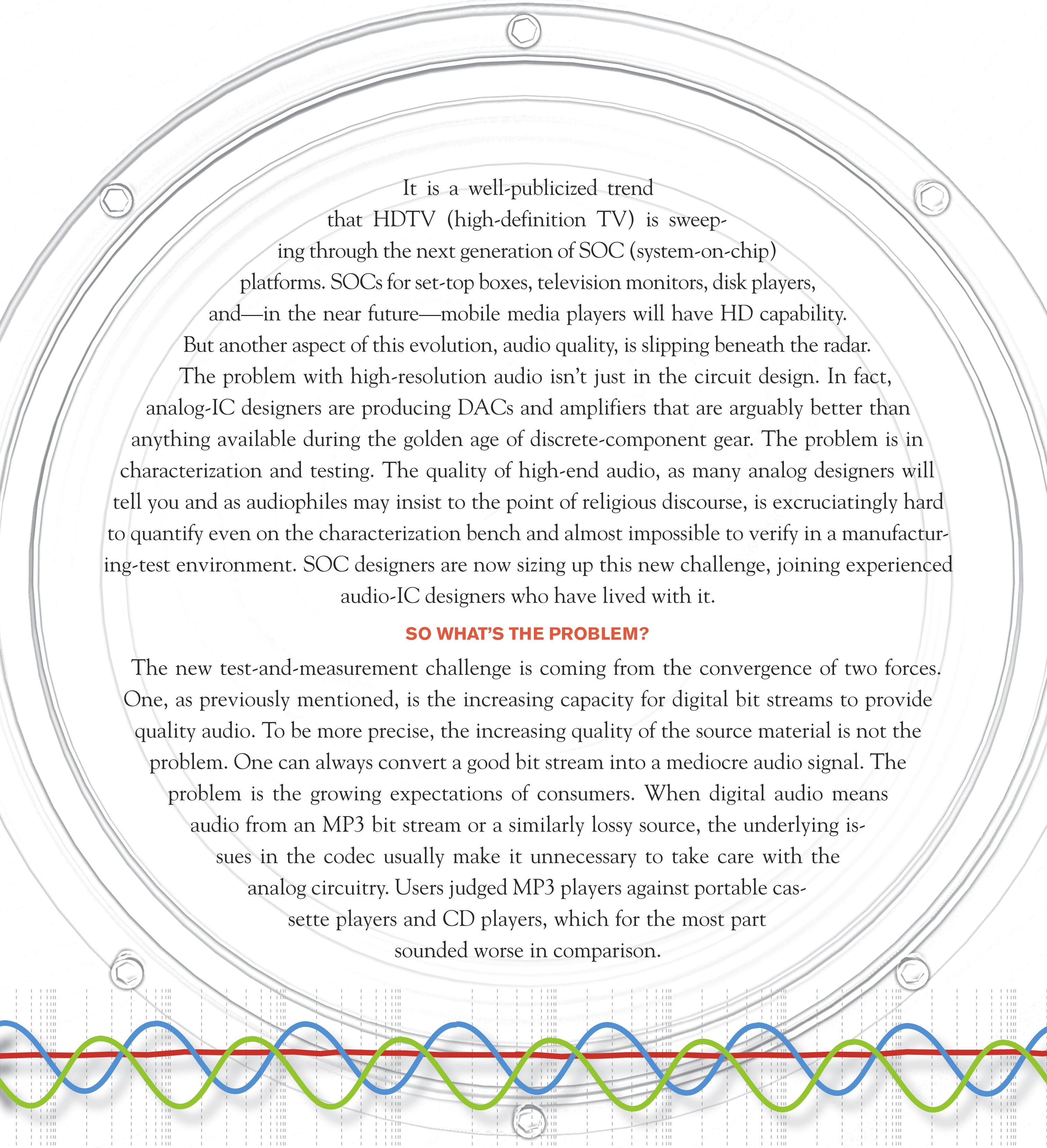
POWER THIS:

testing audio ICs

BY RON WILSON • EXECUTIVE EDITOR

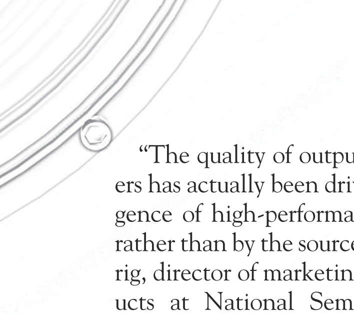
SOCs FOR SET-TOP BOXES, TELEVISION MONITORS, DISK PLAYERS, AND MOBILE MEDIA PLAYERS HAVE OR SOON WILL HAVE HD CAPABILITY. BUT ANOTHER ASPECT OF THIS EVOLUTION—ONE THAT COULD PROVE EVEN MORE CHALLENGING TO SOC DESIGNERS AND TEST ENGINEERS—IS THAT, ALONG WITH HD VIDEO COMES A SIGNIFICANT INCREASE IN THE QUALITY OF THE ACCOMPANYING AUDIO.



It is a well-publicized trend that HDTV (high-definition TV) is sweeping through the next generation of SOC (system-on-chip) platforms. SOCs for set-top boxes, television monitors, disk players, and—in the near future—mobile media players will have HD capability. But another aspect of this evolution, audio quality, is slipping beneath the radar. The problem with high-resolution audio isn't just in the circuit design. In fact, analog-IC designers are producing DACs and amplifiers that are arguably better than anything available during the golden age of discrete-component gear. The problem is in characterization and testing. The quality of high-end audio, as many analog designers will tell you and as audiophiles may insist to the point of religious discourse, is excruciatingly hard to quantify even on the characterization bench and almost impossible to verify in a manufacturing-test environment. SOC designers are now sizing up this new challenge, joining experienced audio-IC designers who have lived with it.

SO WHAT'S THE PROBLEM?

The new test-and-measurement challenge is coming from the convergence of two forces. One, as previously mentioned, is the increasing capacity for digital bit streams to provide quality audio. To be more precise, the increasing quality of the source material is not the problem. One can always convert a good bit stream into a mediocre audio signal. The problem is the growing expectations of consumers. When digital audio means audio from an MP3 bit stream or a similarly lossy source, the underlying issues in the codec usually make it unnecessary to take care with the analog circuitry. Users judged MP3 players against portable cassette players and CD players, which for the most part sounded worse in comparison.



"The quality of outputs for MP3 players has actually been driven by the emergence of high-performance headphones rather than by the source," says Gary Adrig, director of marketing for audio products at National Semiconductor. "As headphones improved, we saw some customers in what had been an undemanding application start to ask for 100-dB SNRs [signal-to-noise ratios] and 0.05% THD [total harmonic distortion]."

As content vendors began to move to lower compression ratios—hence, higher bit rates—chip designers had to move to wider datapaths and better DACs to keep the noise floor of the hardware below the inherent noise level of the decoded source. Despite the limitations of MP3, market competition proved that consumers are quite discriminating about sound quality.

With the new HD media, the pace has picked up as audio tracks have jumped right past CD quality of 16 bits at 44.1k samples/sec to as much as 24-bit, 192k-samples/sec data for DVD Audio. This performance will certainly lead buyers of high-end gear to question the quality of the sound they are hearing. "We are already there in the home-theater market," says Texas Instruments Marketing Manager Kevin Belnap. "Once you reach a minimum level of noise and harmonic distortion, a lot of listener-preference issues, like sound stage and the whole 'vacuum-tube-sound' thing, come into play."

But the critical ear won't stop there. Users of set-top and converter boxes, HD-ready television sets, and even mobile devices are likely to also demand much better audio than they have been hearing. The course of this evolution might be more apparent from one professional-audio developer's experience. Morten Lave, chief executive officer of TC Applied Technologies, a developer of studio-monitor speakers, relates his experience with MP3. "I had an iPod, so I decided to put some music on it," he says. "I used the default settings, and the result was bad; the cymbals sounded awful. So I jacked the bit rate up to 192 kHz. That got me quality as good as the cheap headphones on the iPod, but, if I hook it up to my home system, I can still easily hear compression artifacts." With the new lossless-data types, the electronics will no longer be able to hide behind the limitations of MP3 compression. They will themselves become the issue.

AT A GLANCE

- New digital-media standards are bringing high-fidelity audio to SOC (system-on-chip) platforms.
- High fidelity presents a new kind of characterization problem to SOC designers: one that they can't always solve quantitatively.
- Manufacturing test for these chips will be a gamble based on art and architecture.
- As users' expectations for high fidelity increase, design for test will take on a new importance for audio functions.

This escalating demand for audio quality by itself is manageable. Most SOC vendors in the set-top-box and TV markets, in which space and cost are not draconian overlords, now simply provide a digital output to an external analog chip or chip set. This approach passes the characterization and test problems on to companies in the analog world, which is familiar with them. But the second of two converging forces is closing this loophole for SOC-design teams. That force is integration.

As one SOC vendor puts it, the pervasive demand for greater integration across this market is forcing SOC vendors to put DACs—and later, small power amplifiers—onto the main die. This approach not only dredges up all of the widely discussed problems of precision analog design in a noisy, low-voltage digital-CMOS environment, but also drops the characterization and test problems squarely back in the laps of the SOC team. And it's not going to rest there gracefully.

"We've seen the issues that integration can create," Belnap says. "The early MP3-player guys tried integrating a pulse-width-modulation processor and a DAC onto their chip, but the quality just wasn't there. Now, with HD DVD or Blu-Ray getting integrated into home receivers, we're talking about more challenging integration and a whole new level of sound quality."

HIGH-QUALITY-AUDIO OUTPUTS

You can estimate the problem of characterizing the coming wave of SOCs by comparing the way SOC designers typically characterize analog outputs against the techniques that are emerging at the high end of the audio market. This comparison will result in a rather depressing statement of work for SOC designers. Until recently, SOC characterization has focused on the digital side of the audio problem. Here, standards organizations are more than happy to step in and help, providing source bit streams to stimulate the digital input and references against which to compare the results. In the case of lossy-compression systems, these references are envelopes that define an acceptable range of outputs.

"This started about 10 years ago with Dolby Digital for the ATSC [Advanced Television Systems Committee] and DVD video standards," says Matthew Watson, software-infrastructure manager at Texas Instruments. "They provided results plots for the Audio Precision test equipment, so you could run THD, SNR, and spectral plots and see if you fit."

Among the most assertive in providing such characterization support has been Dolby—for its own codec IP (intellectual property), of course, but third-party organizations, such as THX, have also been active, Watson says. For lossless-audio formats such as CDs, there is no need to provide envelopes—characterization engineers can compare the output bit stream to a reference stream, and standards organizations can insist on bit-exact output. "The digital-output quality is so far above what the analog section can do that our job is basically done when we have met the external standards," Watson says. "Customers understand the rigor of the test procedures, and they accept the results."

But the situation differs greatly on the far side of the DAC. Most chip architects have avoided analog outputs from SOCs, more because of circuit-design and silicon-area issues than testing issues. When architects integrate analog audio, quality expectations have often been low, and characterization has been somewhat perfunctory—examining the analog output at zero and full-scale digital inputs to verify offset and voltage swing and perhaps looking at one output waveform, for instance.

But that situation is changing. As audio moves toward the rarified atmosphere of the audiophile, characteriza-

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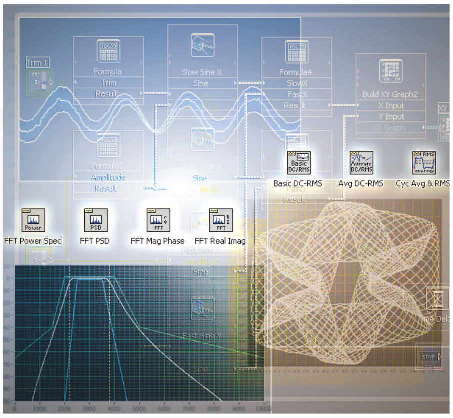

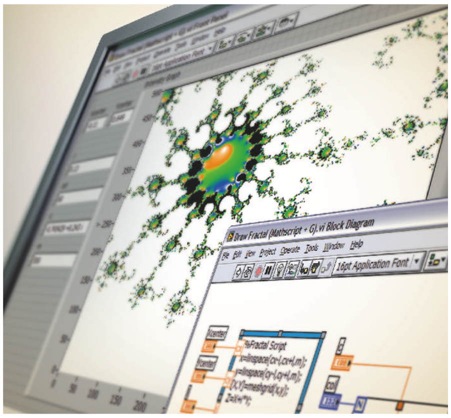

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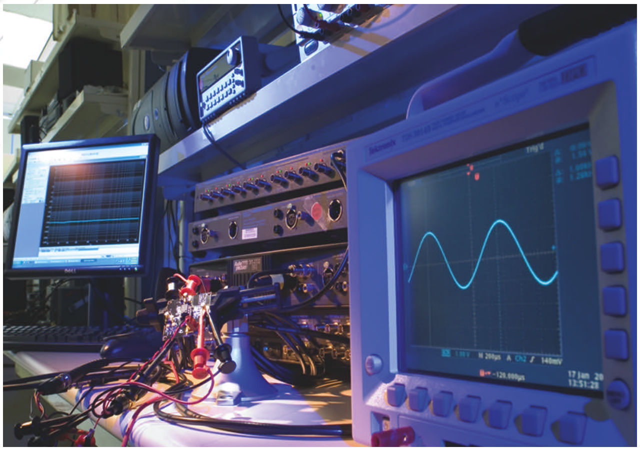

Figure 1 Even simple characterization measurements, such as harmonic distortion, can load up a bench with equipment (courtesy National Semiconductor).

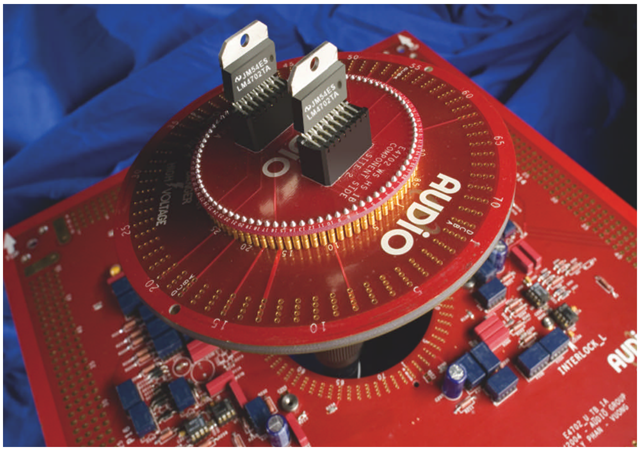

Figure 2 Manufacturing test of high-fidelity-audio outputs involves fixturing, mixed-signal-tester capabilities, and planning beyond what most SOC designers are used to.

tion becomes not only more rigorous, but also more customer-dependent. "At the high end, everyone has a different perspective on the importance of quality," says Julian Hayes, vice president of marketing at high-end-audio-chip vendor Wolfson Microelectronics. "This leads you to a proliferation of characterization procedures." Characterization also becomes harder.

THE ANALOG OUTPUT

Experienced vendors of precision analog break the characterization problem into a number of related questions. What should we measure? How do we make the measurements and under what circumstances? How far do we go? And, in the case of high-end audio, another question looms at the end of the process: Can any amount of measurement give us the right answer? These questions are nontrivial because the goal of characterization is not to determine the electrical performance of the output, but to predict the listening experience. That challenge is far more serious.

Just the question of what to measure turns out to be contentious. For indifferent-quality audio, functional measurements suffice. Frequency response, THD, and some sort of noise measurement are generally enough to determine that an audio section will sound OK to a casual listener through inexpensive headphones. These tests have survived since the early days of high fidelity and are still a starting point. And fortunately for engineers, they all come neatly packaged in a single automated box.

"Everybody has an Audio Precision box these days," says Philippe Mora, director of marketing and business development at Nvidia's newly acquired PortalPlayer division. In recent years, Audio Precision has combined signal generation and acquisition with analysis and PC-based control to become a de facto standard in audio characterization. By combining the hardware with precoded scripts for measurement sequences, Audio Precision has been able to automate not only the traditional audio measurements, but also many of the procedures that third-party standards organizations require.

No one questions the Audio Precision system's ability to deliver accurate measurements, even at the extremes of 24-bit data and 192-kHz sample rates. But some designers also warn that the Audio Precision equipment is only a partial answer. "The AP is our main characterization tool for audio outputs," says Jeff Bridges, audio-applications director at National Semiconductor. "But for specific tests, we will bring in other measuring equipment, as well—usually off-the-shelf tools, like a network analyzer or a spectrum analyzer." This approach has a tendency to give the characterization bench a satisfying mad-scientist look (**Figure 1**). But it can also mean a lot of manual steps in the characterization process.

"The range of characterization procedures we see in the industry now is amazing," suggests Wolfson Chief Technology Officer Peter Frith. "You see some people setting the input to zero and putting a voltmeter on the output to measure noise and then looking at a full-scale sine wave with a scope to measure dynamic range. Others are more traditional: THD, SNR, and dynamic range. But for our markets, that is just the start." Characterization must also include system-related issues. Particular among these is supply-noise rejection, which in itself is hard to even define when the analog output is coming from a chip with substantial digital content and many operating modes. But it can be critical to sound quality.

The fact that SOCs are digital devices with analog outputs creates another category of characterization problems. "Early on, there was no industry standard for click and pop noise in the analog output," says Wolfson's Hayes. "Similarly, the so-called zipper noise that systems can generate as they step through the levels on a digital gain control was new to the audio world. These noise sources, because they come from specific user actions, would never show up on a traditional characterization. But they can be annoying or even injurious if you have a high-performance headphone stuffed in your ear. So, we had to develop characterization tests for them."

THE UNIDENTIFIABLE

But a serious problem remains. "It can happen that an amplifier measures well and just sounds bad," admits TI's Belnap. This statement does not in any way side with what many engineers consider to be a delusional movement among high-end audiophiles—the sort that demagnetizes vinyl records and seeks out hand-braided, gold-plated unobtainium speaker cable. It is rather to admit that the human

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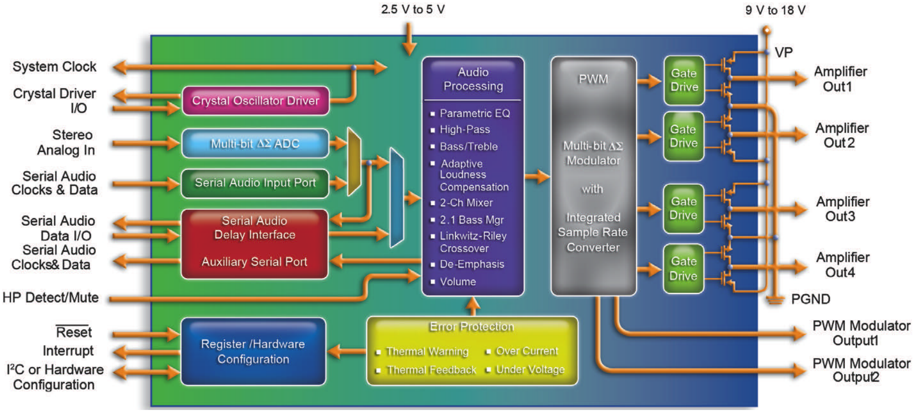

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CS4412	30 W	102 dB	0.1%	4	VP = 9 V to 18 V; VD = 2.5 V to 5 V	Quad Power Stage IC Thermally Enhanced 85% Efficiency	48 QFN
CS44130	60 W	107 dB	0.12%	4	VP = 10.8 V to 21 V; VD = 3.3 V or 5 V; VL = 2.5 V to 5 V	Quad Power Stage IC Thermally Enhanced 90% Efficiency	48 QFN
CS44600	N/A	100 dB	<0.05%	6	VD = 2.5 V; VL = 3.3 V to 5 V	192 kHz Digital Amplifier Controller	64 LQFP
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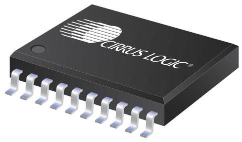

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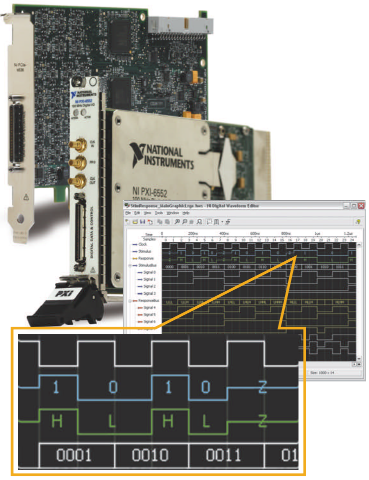

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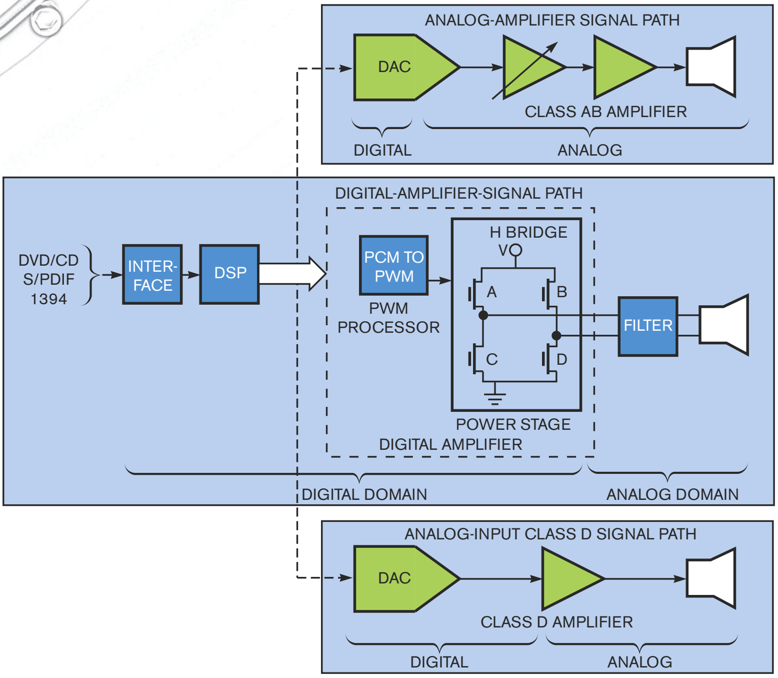

Figure 3 Designers must be able to observe a variety of signal paths to characterize and troubleshoot mixed-signal-audio outputs.

ear is sufficiently sensitive and adaptable that there is no one quantitative test that can predict how a given DAC, amplifier, and speaker combination will sound to experienced listeners.

This reality has already struck high-end-audio-IC vendors. “At the high-performance end of our market, we used to walk in with sample parts and spec sheets and show customers the data,” relates National Semiconductor’s Bridges. “But recently, more customers have been asking us to leave the spec sheet at home and bring in a working reference design. They take it right into their sound room and start listening to it. At the high end today, quality is all about how the chip sounds.”

This situation presents some obvious problems. For one thing, the fixtures designers use for characterization are often poor representations of a real listening environment. “Almost everyone does their data sheets based on resistive loads,” Bridges observes. But only a very stable amplifier behaves in the same way with a resistive load as it does with a dynamic, reactive load, such as a loudspeaker. In fact, TC Applied Technologies’ Lave suggests that at least for Class D and fully digital amps, the problem of controlling the speaker cone—or, ultimately, the sound-pressure level on the surface of the cone—is sufficiently speaker-dependent that active speakers—those with dedicated built-in amplifiers—will predominate in the industry. It’s simply too hard to build an amplifier that can control all the dynamics that any conceivable speaker network can throw at an output stage.

That problem is not the last one, either. Interacting with skilled listeners often uncovers audible issues that are perfectly measurable—if you know what you are looking for (see **sidebar** “Can you even measure that?” at the Web version of this article at www.edn.com/070301cs). Some listener observations that sound totally irrational turn out to be not only reproducible in blind tests, but also traceable back to something that actually does show up in measurements. Each one of these experiences adds its own contribution of complexity to the characterization process.

The result is a characterization process that tends to produce a “sound” that listeners begin to associate with a manufacturer. In some cases, vendors strive to make the sound as dry, or neutral, as possible. “We aim for a dry sound—as much as possible consistent with the price point,” says TI Senior Applications Engineer Fred Shipley. “That allows our customers to manipulate both

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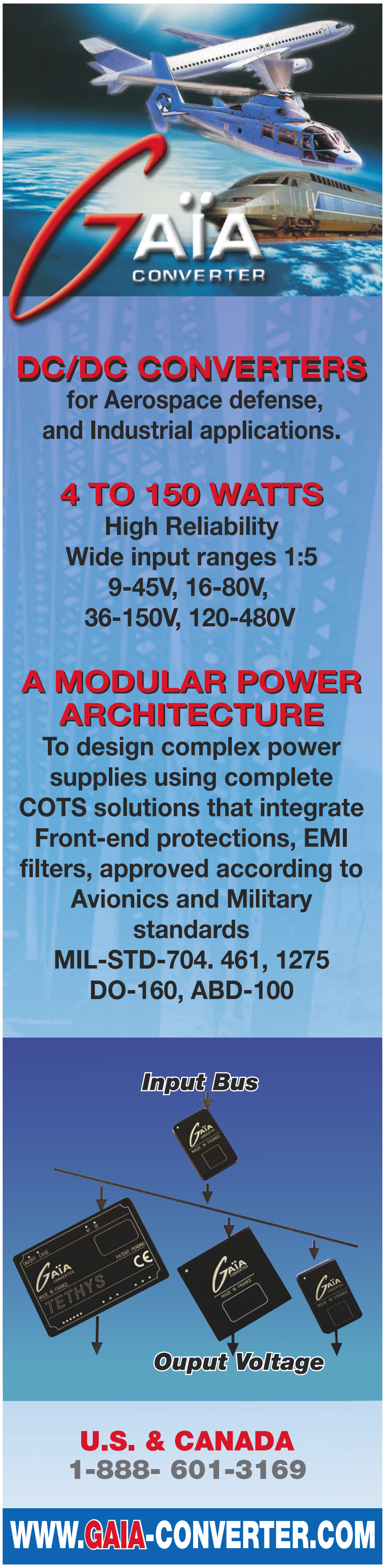

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their digital-signal processing and their board-level analog design to create their own characteristic sound, rather than having to work with ours." Shipley adds that part of the process of characterizing chips for this TI dry sound is a significant amount of time in the listening room, exposing the chips in TI's reference design to the company's golden ears.

When the SOC *is* the board-level design, the responsibility for the ultimate sound falls on the chip designers. And that sound may be more market-related than specification-based. PortalPlayer's Mora observes, "You need empirical testing, as well. What's 'right' to listeners depends, among other things, on their culture and listening habits. For instance, as a generalization, Asian markets tend to prefer emphasis on the higher frequencies in the spectrum. Europeans tend to think a flatter frequency response but more volume sounds more natural."

So in the end, is characterization quantitative or qualitative? "I subscribe to both sides of that debate," says Bruce Hofer, chairman and co-founder of Audio Precision. "On the one hand, things can happen that are audible but don't show up in a typical characterization procedure. Take, for instance, PC sound cards. Traditional measurements might say that a card performs splendidly but would never tell you that, when the PC is busy, the software will miss a deadline and cause a dropout that is very audible to listeners. On the other hand, I really want to believe that if something is audible, we should be able to measure it somehow. It takes measuring and listening."

MANUFACTURING TEST

If characterization is such a complex question, manufacturing test in the SOC world promises to be a nightmare. "The key issue here is that you are trying to ensure the quality of a part, and you have a total of 5.5 seconds of test time," explains Marcel Tromp, engineering fellow at LSI Logic. That total time budget is insufficient to complete some of the individual tests that are routine on the characterization bench, let alone thoroughly test an analog output. And one home-theater SOC might have nearly a dozen outputs. Add to this problem the realities of the manufacturing-test environment and the variety of customer-test requirements. "Some customers nearly ignore the ability of the chips to deliver fantastic audio quality; they just don't care as long as the output is functional," laments Wolfson's Frith. "And then there are others, like the Japanese systems manufacturers and the automotive industry, who test everything," adds Hayes. "We have some customers who just have a scope on the end of their production line and others who measure every incoming chip with an Audio Precision box."

Just performing manufacturing tests is becoming a challenge (**Figure 2**). Frith says that testing analog from a 24-bit, 192k-sample source can take all of the dynamic range—and, more challenging, all of the noise margin—of which the best Teradyne mixed-signal testers are capable. And the paucity of high-dynamic-range signal cards can mean that engineers will test analog outputs sequentially, rather than in parallel groups. But even this problem may not be the most serious one. "At this level, there is a trend for the R&D department to specify the whole test environment," Hofer says. "But that becomes difficult in today's world of third-party testing houses where distance and culture are barriers. In China, I've seen facilities in which you couldn't count on the third wire for the test systems' actually being grounded anywhere." This news is dreadful for an environment that is high in electrical noise under the best circumstances.

So test design becomes an art. Characterization engineers must work with test engineers to find a minimum number of tests—of which the real-world test equipment will be capable within the time budget—that will provide a high probability that the chip will sound as the customer expects. Only experience, a thorough knowledge of audio, and

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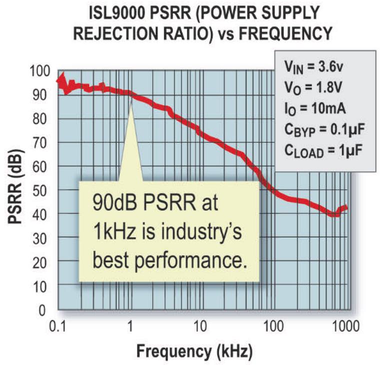

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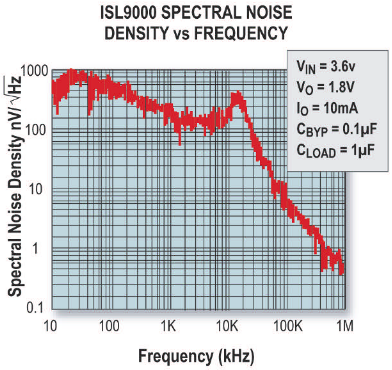

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good luck can achieve that. “Defining a set of quantitative tests is becoming a skill set in its own right,” LSI’s Tromp says. “How do you bring nonquantitative ideas of good and bad into the engineering world? It’s much the same problem as in video, where the ultimate judge is the viewer. But, at least in video, if something doesn’t look right, you can stop the frame and examine it.”

There are some hints from the experts, though. “The majority of test problems come down to routing and accessibility,” Hofer declares. “Accessibility is key. For instance, if you have an on-chip DAC, you need to be able to get to both sides of it. Otherwise, you are just measuring the subsystem end to end with no idea of what’s going on inside.”

This issue makes design for accessibility a critical skill for high-end audio. Engineers need to bring test points out of the SOC. But the routing of these test signals is every bit as critical as the routing of the real analog output, or the data will be nearly useless. Crosstalk, an analog multiplexer with a high noise floor, and any number of things that seem unimportant can destroy the visibility into an analog node when you are making measurements with 110-dB dynamic range.

Ironically, a concept from digital self-test may be important here, as well: structural, as opposed to functional, test. Given that there simply won’t be enough time to fully test the function of a precision-audio output, the designer must understand the likely failure modes and design the chip to help inspect for them. “We are fairly fortunate in that our stuff is digital until it hits the second-order filter,” says TI’s Shipley of the company’s Class D amplifiers (**Figure 3**). “But even so, we have to relate what is happening in the analog signal back to the digital architecture, based on our understanding of the circuit. The tester looks at switching waveforms on the die, and you have to be able to know how that impacts the sound the customer will hear.”

In the end, manufacturing-test procedure becomes a cooperative effort between the SOC designer and the test system. Perform a few specific tests with the test system and find out how this chip will sound driving a pair of headphones or a Class D amplifier from Brand X. It’s no small challenge, but with listening rooms the ultimate arbiters of quality at the high end of the audio world, it’s a challenge that SOC design and test engineers must face.**EDN**

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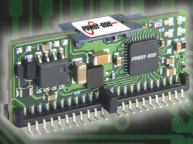

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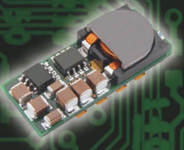

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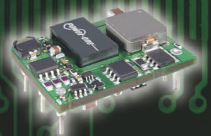

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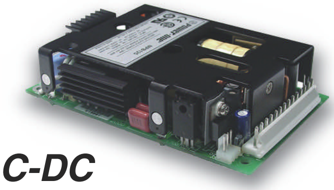

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Comparing dc/dc converters' noise-related performance

NOISE IN DC/DC CONVERTERS CAN DIFFER FROM DEVICE TO DEVICE. AN UNDERSTANDING OF THE MAIN DC/DC-CONVERTER TOPOLOGIES AND THEIR NOISE-PERFORMANCE DISPARITIES CAN HELP.

Today, dc/dc-converter components employing high-frequency switching are the devices that designers most often use to accomplish power conversion. Designers have long recognized efficient high-frequency operation as the key to achieving high power density and improved performance in switch-mode converters. High-frequency operation translates into smaller magnetics and capacitors, shorter response times, smaller filters, and lower noise levels. Notwithstanding noise-performance improvements, all dc/dc converters generate EMI (electromagnetic interference), or noise. This noise—common mode, differential mode, and radiated—can vary widely among dc/dc converters from supplier to supplier and topology to topology. Although the many designs, or topologies, of dc/dc-converter components number in the hundreds, two are dominant: so-called fixed-frequency PWM (pulse-width-modulation) and variable-frequency, quasiresonant ZCS/ZVS (zero-current switching/zero-voltage switching). Design engineers working with dc/dc converters must understand the noise performance differences of these two main topological classes.

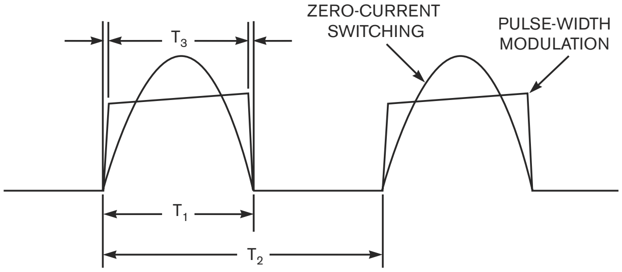
Fixed-frequency PWM converters inherently trade off efficiency against operating frequency because of switching losses. These converters dissipate power and noise in the switching element each time they discontinuously make and break inductive-current flow during their brief turn-on and turn-off transitions. Power dissipation due to switching losses increases directly with operating frequency in PWM converters until it becomes a dominant loss factor. At that point, efficiency declines rapidly, and the thermal and electrical stresses on the switch element become unmanageable. The losses result in a "frequency barrier" that limits achievable power density in conventional converters.

Variable-frequency, quasiresonant ZCS/ZVS converters overcome the frequency barrier by implementing forward-converter switching at zero current and zero voltage. Each switch cycle delivers a quantized "packet" of energy to the converter output, and switch turn-on and turn-off occurs at zero current and voltage, resulting in an essentially lossless switch. ZCS converters can operate at frequencies in excess of 1 MHz. By eliminating the fast current discontinuities characteristic of conventional topologies, ZCS/ZVS results in a virtually lossless transfer of energy from input to output with dramatically reduced levels of conducted and radiated noise.

The noise that the switch generates is a major difference between PWM and ZCS/ZVS converters. Among other differences, ZCS/ZVS converters have sinusoidal waveforms rather than the square waveforms of PWM converters. The lower harmonic content and lack of sharp edges of ZCS/ZVS result in much less excitation of parasitic capacitance and inductance, resulting in less noise. With PWM, the input voltage switches at a constant frequency—usually, several hundred kilohertz—to create a pulse train. The converter adjusts the width of the pulses to provide the necessary power to the load at the correct voltage. At full load, the current waveform looks much like a square wave (**Figure 1**).

Many designers intuitively assume that it's easier to design a filter for a fixed-frequency converter than for a variable-frequency converter. In fact, the opposite is true (**Reference 1**). The perception is, in all likelihood, attributable to the term "fixed frequency," which is a misnomer. Both topologies have frequency elements that are more or less fixed and frequency elements that vary as a function of operating conditions.

Figure 1 compares the waveforms of the current flowing through the main switch. In a module using a quasiresonant



NOTES: PULSE-WIDTH-MODULATION CONVERTERS OPERATE AT A LOWER FREQUENCY THAN ZERO-CURRENT-SWITCHING CONVERTERS.
T_1: ON-TIME OF THE SWITCHING DEVICE.
T_2: PULSE-REPETITION RATE OR OPERATING FREQUENCY.
T_3: RISE AND FALL TIME OF THE CURRENT ON THE SWITCHING DEVICE.

Figure 1 ZCS/ZVS converters have sinusoidal waveforms rather than the square waveforms of PWM converters. The lower harmonic content and lack of sharp edges of ZCS/ZVS result in much less excitation of parasitic capacitance and inductance, resulting in less noise. Not drawn to scale.

topology, the pulse width or on-time, T_1, is fixed, and the repetition rate or period, T_2, is variable. Conversely, in a module using PWM, the opposite is true; the repetition rate is fixed, and the pulse width is variable. The rise/fall time, T_3, is a fixed frequency in both topologies. In the variable-frequency design, however, there are no high-frequency components associated with the leading and falling edges of the current waveform, T_3, because it is essentially a half-wave-rectified sine wave. The spectral content of the variable-frequency waveform is lower in amplitude and contained in a narrower band. **Figure 2** shows the characteristic harmonic spectra for each of the topologies. In the fixed-frequency waveform, the spectral content is higher in amplitude and spread over a broader range of harmonics.

A more difficult aspect of converter EMI to control is that of parasitic excitation by high di/dt in PWM converters. This excitation results in noise of 10 to 30 MHz, which can be difficult to suppress because it often couples to the secondary of the converter through the transformer as common-mode noise. ZCS/ZVS converters generate less parasitic noise due to the "soft" edges of the current waveform. **Figure 3** shows a typical comparison.

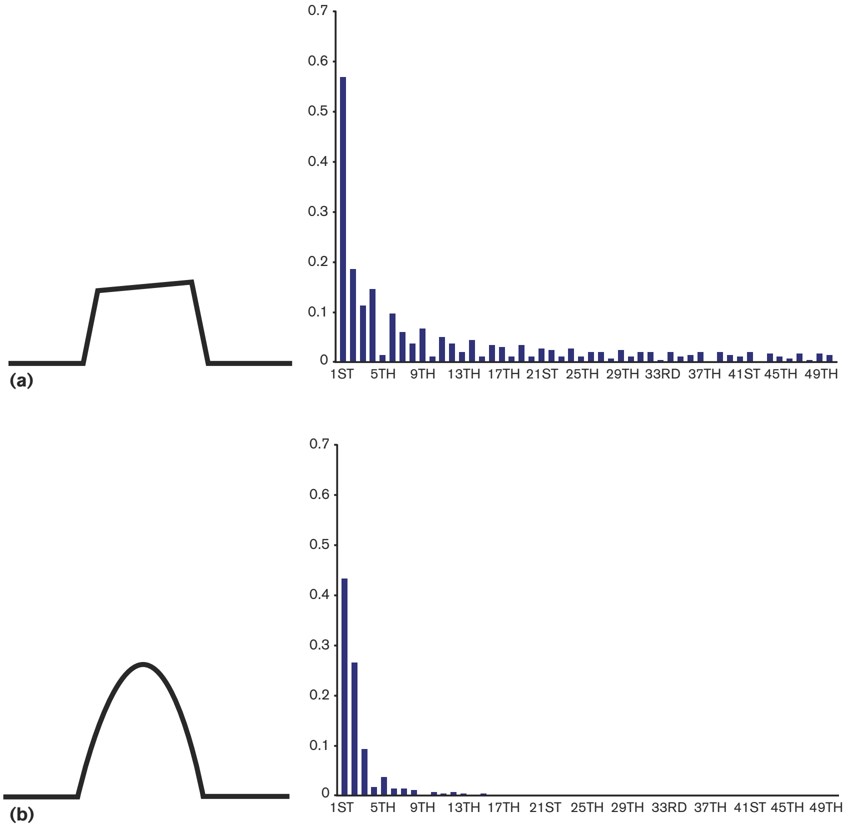
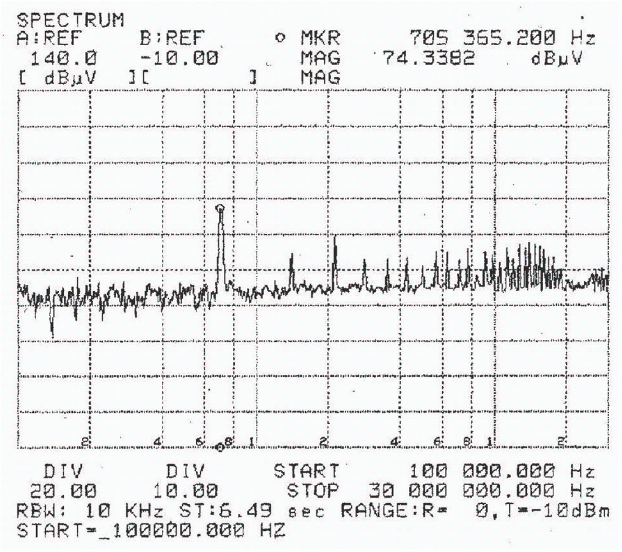


Figure 2 The spectral content of the fixed-frequency waveform (a) is higher in amplitude and spread over a broader range of harmonics, whereas the spectral content of the variable-frequency waveform (b) is lower in amplitude and contained in a narrower band. Note: The waveforms are not drawn to scale.

Clearly, for applications that require low noise, an effective first step to minimizing noise that the dc/dc converter generates is to select a topology, such as ZCS, that is inherently lower in common-mode noise. Also, designers should avoid using some products in noise-sensitive applications. Control devices mounted on copper plates, for example, create parasitic capacitance from primary-referenced control devices to secondary-referenced control devices through the copper base, resulting in high common-mode noise. Incidentally, even for applications that need not meet EMI requirements, designers typically use bypass capacitors at the input and the output pins of dc/dc converters because they are the most effective way to reduce common-mode noise. **Figure 3** shows an example of conducted input noise of a dc/dc converter—in this case, a variable-frequency, quasiresonant ZCS dc/dc converter using bypass capacitors but with no additional filtering.

Although component power modules usually incorporate some internal input and output filtering, designs often need additional external filtering to meet either system requirements or agency specifications. For example, FCC (Federal Communications Commission) and European agencies specify the allowable levels of power-supply noise that may conduct back into the ac line. Many designers tackle these issues on their own, but most dc/dc-converter manufacturers provide detailed application notes and offer the assistance of a knowledgeable,



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SPECTRUM
A:REF     B:REF         o MKR      705 365.200 Hz
 140.0    -10.00          MAG     74.3382     dBμV
[ dBμV   ][           ]   MAG

 DIV        DIV        START       100 000.000 Hz
 20.00      10.00       STOP   30 000 000.000 Hz
RBW: 10 KHz ST:6.49 sec RANGE:R=  0,T=-10dBm
START=_100000.000 HZ
```

Figure 3 The spectral density of the conducted noise versus load appears for a 48V-input, 5V-output, 30A-load ZCS dc/dc converter using bypass capacitors but no additional filtering.

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experienced, and accessible application-engineering staff. Some dc/dc-converter suppliers also offer ac front ends and EMI filters as modular accessories. These filters not only save time, but also provide a means of risk prevention. The EMI filter works with the supplier's converter modules, and, assuming proper layout, the combination meets the specified EMC (electromagnetic-compatibility) directives.

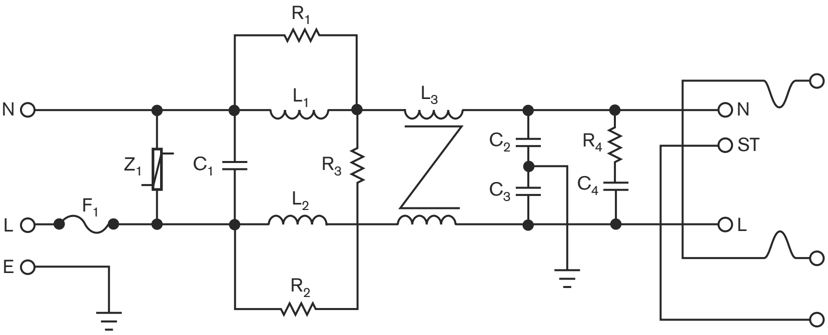

Figure 4 This filter configuration provides sufficient attenuation to comply with the Level B conducted-emissions limit for emission noise standard EN55022. The single-package EMI filter comprises a through-hole filter with a common-mode choke and Y capacitors between line and ground, plus two additional inductors and an X capacitor between the two lines. Z_1 provides transient protection.

In the United States and Europe, the Class A and Class B limits of both FCC and VDE (Verband der Elektrotechnik, www.vde.com/vde_en) standards govern conducted-noise emissions. In the United States, the FCC requires compliance with Class A for equipment operating in factory settings and Class B, the stricter standard, for equipment for home use. In Europe, all countries require that equipment for both home and factory use meets the VDE Class B standard.

Most switching power supplies today operate at 100 kHz to 1 MHz. Usually, the dominant peaks in the conducted-noise spectrum reflect back to the power line and correspond to the fundamental switching frequency and its harmonic components. Conducted-emissions standards, such as EN55011 and EN55022, set quasipeak and average limits on conducted noise from the input of converters or power-supply systems back to the source over the frequency range of 150 kHz to 30 MHz. To comply, all of the conducted noise—the peaks in the spectrum—must fall below the specified limits.

Designers most often construct EMI filters in a single package with configurations similar to that of **Figure 4**. The through-hole EMI filter has a common-mode choke and line-to-ground Y capacitors plus two additional inductors and a line-to-line X capacitor. Z_1 provides transient protection. This filter configuration provides sufficient attenuation to comply with the Level B conducted-emissions limit. **Figure 5** shows a comparison of ZCS-converter-generated and PWM-converter-generated conducted-input noise. Notice that the unfiltered noise performance of the ZCS converter in **Figure 3** is superior to the filtered noise performance of the PWM converter.**EDN**

REFERENCE

[1] Hsiu, L, M Goldman, R Carlsten, A Witulski, and W Kerwin, "Characterization and Comparison of Noise Generation for Quasi-Resonant and Pulsewidth-Modulated Converters," *IEEE Transactions on Power Electronics*, Volume 9, No. 4, July 1994.

AUTHOR'S BIOGRAPHY

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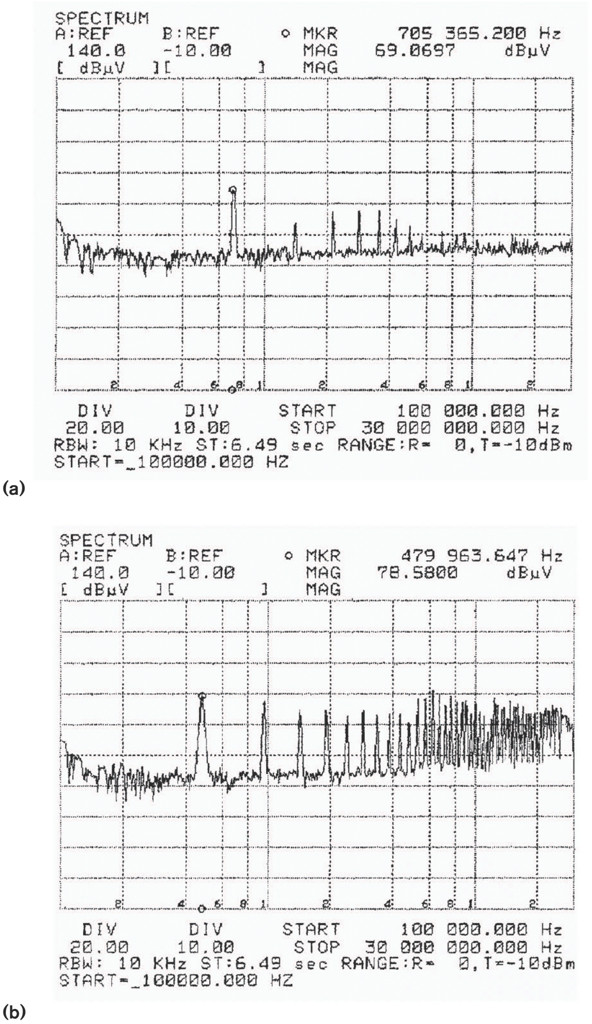

Figure 5 The conducted input noise for a ZCS converter with a common-mode choke (a) and for a PWM converter with a filter (b) are both for a 48V-input, 5V-output, 30A converter.

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Optimizing handsets' multimedia connectivity and performance

BOTH CONSUMER DEMAND AND COMPETITIVE PRESSURES ARE DRIVING THE RAPID PROLIFERATION OF HANDSETS' MULTIMEDIA CAPABILITIES. IN STRIVING TO INTEGRATE THE NECESSARY PERIPHERALS, CELL-PHONE ARCHITECTS AND DESIGNERS MUST MAKE INFORMED FEATURE TRADE-OFFS WHEN EXPLORING ARCHITECTURE OPTIONS.

One of the fundamental requirements of a multimedia handset is the ability to handle high-bandwidth transfers of large audio, image, and video files. This multimedia content downloads to the handset either through the mobile network or through a PC, and the embedded and removable nonvolatile storage within the handset houses it. The handset's main CPU, which can be either a standalone baseband processor or a combination of a baseband and an applications processor, handles functions such as wireless communication and the operating system, whereas dedicated peripheral controllers often facilitate the data-intensive multimedia transfer from PC to mass storage.

PC CONNECTIVITY

Several options exist for multimedia connectivity between a handset and a PC, including Bluetooth, IrDA (Infrared Data Association), FireWire, USB, and Wi-Fi (**Table 1**). However, few of these mechanisms provide support for high-speed data transfers with the ease and flexibility that end users demand. With a raw throughput of 480 Mbps and wide adoption across PCs as a plug-and-play option, High-Speed USB is best able to meet these requirements. For example, under real-world operating conditions, it takes approximately 13 minutes to transfer 128 Mbytes (approximately 27 songs) from a computer to a handset using Full-Speed USB. The same transfer using High-Speed USB takes less than 30 seconds.

A typical High-Speed USB system must contain several standard components. Endpoint buffers, for example, store USB data. Other common building blocks include an SIE (serial-interface engine); a USB-transceiver PHY (physical layer); program memory for the USB-software stack; and configuration, status, and control registers. As noted, the endpoint buffers store all USB data and are usually structured in a FIFO (first-in-first-out) architecture. The SIE sends data to and receives data from the endpoint buffers. It detects and creates the standard USB-packet signals; it also encodes and decodes USB data residing on the parallel bus that communicates with the PHY. The PHY, an analog switch, is the hardware interface between the parallel bus of the SIE and the serial lines of the USB connector.

The proliferation of multimedia-file downloads to the handset drives the ever-increasing need for mass storage on the handset. This storage may be embedded, such as SLC (single-level-cell) and MLC (multilevel-cell) NAND flash memories, along with CE-ATA (Consumer Electronics-Advanced Technology Attachment) hard drives or removable SD (Secure Digital) cards and MMCs (Multimedia Cards).

INTEGRATING HIGH-SPEED USB

The analog PHY can be discrete and, therefore, external to the digital-dominant SIE, endpoint buffers, and USB registers. If the baseband or applications processor integrates the SIE and endpoint buffers, the PHY is always external because the USB PHY is analog in nature, preventing it from scaling, as well as digital when moving down the technology-geometry curve

TABLE 1 HANDSET-CONNECTIVITY OPTIONS

	Wireless				Wired		
Consideration	**Bluetooth 1.2**	**Bluetooth 2.0**	**Wi-Fi 802.11g**	**SIR-LP IrDA**	**FireWire**	**USB 1.1**	**USB 2.0**
Usage model	Point-to-multipoint	Point-to-multipoint	Point-to-multipoint	Point-to-point	Repeater-based	Tiered star	Tiered star
Maximum data rate	1 Mbps	3 Mbps	54 Mbps	115 kbps	400 Mbps	12 Mbps	480 Mbps
Power	Low	Low	High	Low	Low	Low	Low
PC adoption	Medium	Medium	Medium	Very low	Low	Very high	Very high

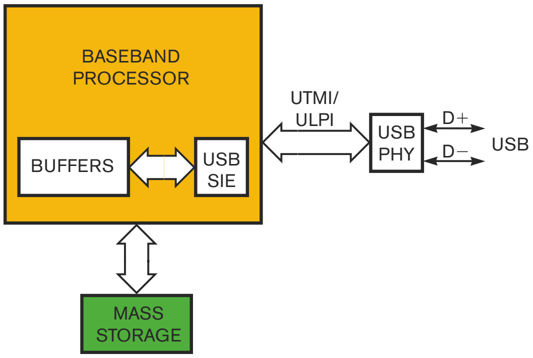

Figure 1 If the main processor integrates the USB SIE, only the PHY must be external.

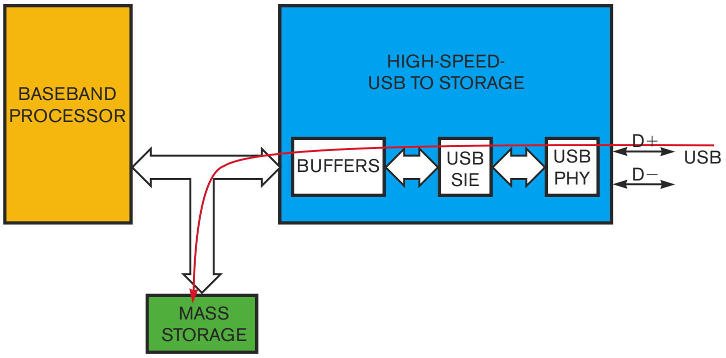

Figure 2 A High-Speed USB-to-mass-storage direct connection complicates simultaneous access by the processor.

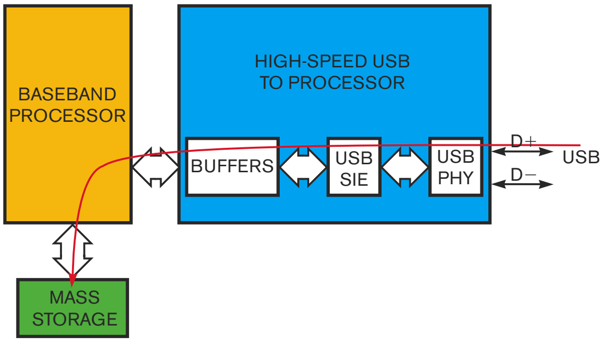

Figure 3 Using the CPU as an intermediary between the High-Speed USB transceiver and mass storage incrementally burdens the processor.

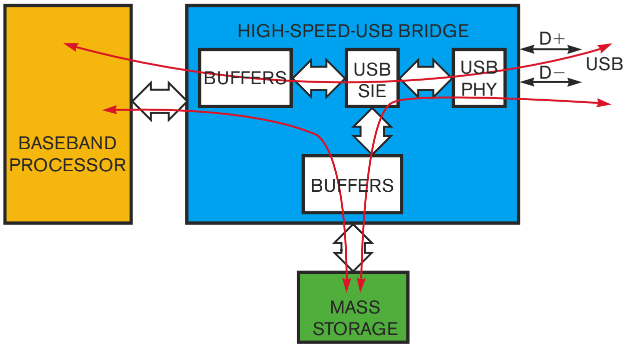

Figure 4 A bridge approach addresses the downsides of the alternatives but at the trade-off of a larger system, greater power consumption, and a higher price.

from 90 to 65 nm and beyond. Most handset processors integrate Full-Speed USB SIEs, but a few integrated High-Speed USB SIEs exist. In the rare cases of integrated High-Speed USB SIEs, the designer must select an external High-Speed USB PHY (**Figure 1**).

A designer can choose from two types of High-Speed USB PHYs; the high-speed interface that connects the processor to the PHY guides the selection process. The two most common processor-to-PHY interfaces are UTMI (USB 2.0 Transceiver Macrocell Interface) and the more recent ULPI (UTMI-plus-low-pin interface). UTMI requires 22 to 26 pins. ULPI reduces this pin count to between eight and 12, which also reduces the overall pin count of the High-Speed USB PHY.

With a baseband or applications processor that does not integrate the High-Speed USB SIE, the handset must instead integrate the endpoint buffers, SIE, and PHY into a companion chip. Three main types of devices accomplish this task; the first converts High-Speed USB data directly into mass-storage data. This type of configuration allows for a single-step transfer of large files received across the High-Speed USB port. The processor and the USB-to-mass-storage device share the mass-storage bus, and only one device can access the bus at any time (**Figure 2**).

This approach potentially creates several issues. For example, consider a scenario in which the baseband processor receives a phone call and needs to retrieve a ring tone from mass storage while the USB-to-mass-storage device is downloading data from a PC. Because only one device has access to the mass-storage bus at a time, the phone communication cannot happen while data is downloading and vice versa. Such an approach has its benefits in certain circumstances, however. Because the device has a direct path to mass storage, PC-to-mass-storage transfers are optimized for performance. Also, the approach minimizes software overhead on the processor side to handle USB transfers. And, in the case of NAND-flash-memory-based or similar mass storage, the High-Speed USB controller may handle all of the wear leveling, bad-block management, and ECC (error-correction coding) associated with USB transfers, thus simplifying the overall design.

The second approach uses a High-Speed USB-to-processor device that sends information to the baseband processor, which then relays it to mass storage (**Figure 3**). Software interleaving on the processor must allow for concurrent transfer of data to mass storage from the PC, along with other handset functions. In this configuration, the datapath from the PC to mass storage is indirect. This configuration also incurs more software overhead, reducing the maximum achievable bandwidth from the PC to mass storage.

Every High-Speed USB data transfer must pass through the processor, thus burdening limited processor resources. This approach does address the issue of simultaneous communication to mass storage. However, it does so at the cost of reducing overall High-Speed USB transfer speeds and consuming processor resources.

Alternatively, the use of a bridge provides a direct path from

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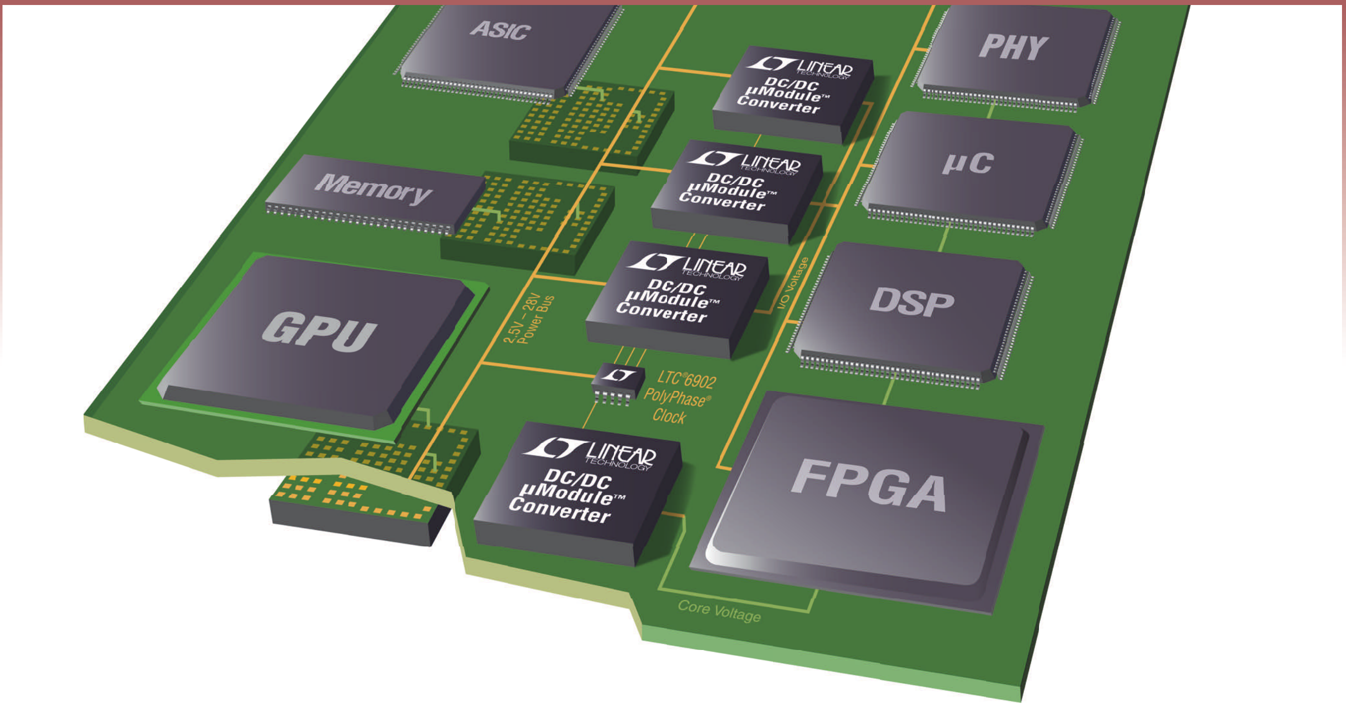

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LTM4603	6		✓	✓	✓		
LTM4603-1	6		✓	✓			
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LTM4601	12		✓	✓	✓		
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LINEAR TECHNOLOGY

High-Speed USB to mass storage while allowing the processor to access mass storage (**Figure 4**). This approach must maintain multiple endpoint buffers: one group for communication from High-Speed USB to mass storage and processor to mass storage, as well as another group for communication between the processor and High-Speed USB. These distinct endpoint buffers are necessary to allow for independent transfers of information between the three ports.

In this approach, the processor has no involvement in the transfer of large data files from the PC to mass storage, thereby reducing transfer latency, increasing transfer speed, and reducing the load on the main processor. Additionally, using the three independent ports of the bridge allows for simultaneous usage models. For instance, the handset can now connect to the PC as a modem while downloading multimedia from the PC. The primary trade-off of the bridge approach is increased cost and size, due to additional logic and endpoint buffers. The additional simultaneous-usage models may also lead to an increase in power consumption.

ASSESSING THE ALTERNATIVES

Without a doubt, High-Speed USB is a must-have connectivity option for large-payload downloads from a PC. However, multiple implementation approaches exist. The application throughput, usage model, and handset-system requirements determine the best High-Speed USB implementation approach in each situation.

Handsets that have processors with built-in High-Speed USB SIEs can take advantage of this high level of integration and choose the PHY based on the type of High-Speed-USB interface the processor has: UTMI or ULPI. In all other cases, developers must balance performance, user experience, software overhead, power, package size, and cost to determine the optimum approach. External USB-to-storage or USB-to-processor options minimize cost, size, and power consumption but have reduced data throughput and processor performance compared with a bridge approach. Employing a bridge maximizes throughput, minimizes processor intervention, and enables simultaneous-usage models yet typically requires a larger package, greater power consumption, and increased price.**EDN**

AUTHORS' BIOGRAPHIES

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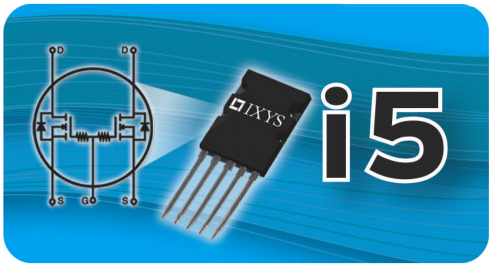

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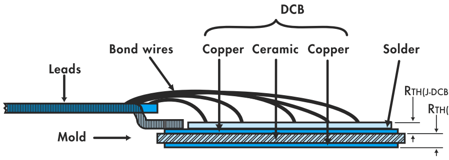

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IXTL2x240N055T	55	240	140	4.4	170	30	1.0	1
IXTL2x220N075T	75	220	120	5.5	165	50	1.0	1
IXTL2x200N085T	85	200	112	6.0	152	55	1.0	1
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Small, high efficiency DC/DC converters are critical to the design of leading-edge electronics. Achieving high accuracy and efficiency traditionally means adding extra components, complexity, and size. Not so with the LT3837. This flyback controller serves 10W to 60W isolated applications with high performance, simplicity, small size, and a minimum component count.

High-Efficiency Controller Capabilities

The LT®3837 operates from a 4.5V to 20V input, but the converter input range can be extended upwards by using a V_{CC} regulator and/or a bias winding on the transformer. It also provides a synchronous rectifier output with adjustable timing to optimize efficiency and enhance cross-regulation in multiple-output supplies.

The LT3837 eliminates the need for the traditional secondary-side reference, error amplifier, and optoisolator circuits by sampling the flyback voltage on a primary-side winding. Accuracy is enhanced with output resistance compensation. Current mode control with leading edge blanking yields a high performance loop that is easy to compensate.

The operating frequency is adjustable from 50kHz to 250kHz or can be synchronized to an external clock. Soft-start provides well controlled start-up with limited inrush current. Protection features include current limit with soft-start cycling for severe overloads, undervoltage lockout, and thermal shutdown.

3.3V, 10A Converter Operates from a 9V to18V Source

The circuit shown in Figure 1 is a flyback design for a 3.3V, 10A output from a 9V to 18V input with a minimum of external components. The LT3837 samples the voltage on the primary winding during the flyback interval to provide superb regulation. Figure 2 shows ruler-flat regulation at 9V input, and a tight regulation window of ±0.7% over line and load. Synchronous rectification with adjustable

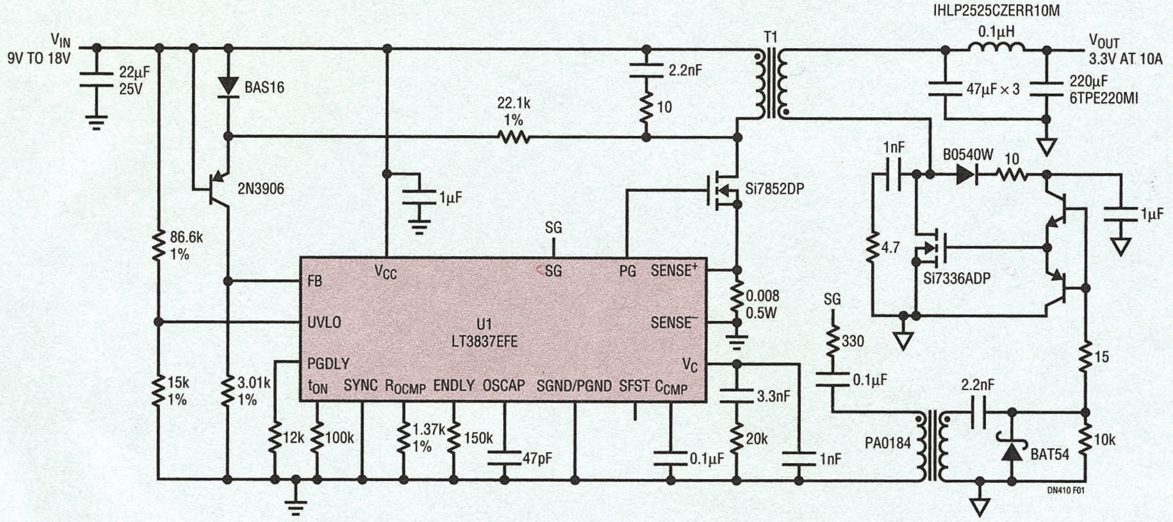

Figure 1. Low Parts Count, 9V to 18V Input to 3.3V/10A Output Isolated Flyback Converter with ±0.7% Regulation

---

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timing yields excellent efficiency—88% over a wide range of operating conditions—as shown in Figure 3.

3.3V, 10A Converter Operates from a 9V to 36V Source

Figure 4 shows an enhanced circuit that extends the input operating range of the LT3837 to 9V to 36V. Operation is converted to hysteretic start-up for efficient wide-range operation. Q1 provides a low-drop current source for start-up, and Q2 creates a suitable undervoltage circuit for V_{CC}. These circuits, together with the V_{CC} winding on the transformer, result in low V_{CC} power at higher input voltages and low dissipation cycling when operating into a short circuit. This circuit is implemented in a 1.5in^2 footprint. This circuit exhibits excellent regulation of ±1.2% over line and load, and efficiency of 88% over much of its operating range.

Conclusion

The LT3837 is part of a new class of flyback controllers developed by Linear Technology to satisfy the demand for economical, high performance power converters. It provides synchronous rectifier drive and eliminates the need for secondary regulation circuits and optoisolators. The LT3837 makes it easy to implement high performance Flyback designs that are cost effective, small and efficient.

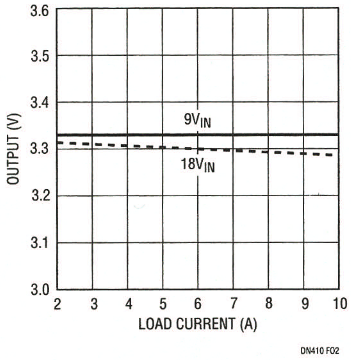

Figure 2. Regulation of the Converter in Figure 1

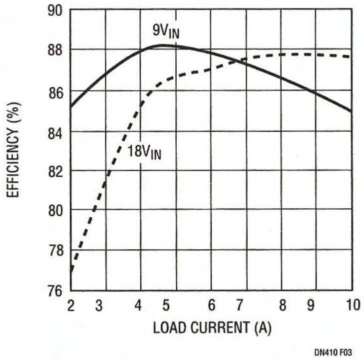

Figure 3. Efficiency of the Converter in Figure 1

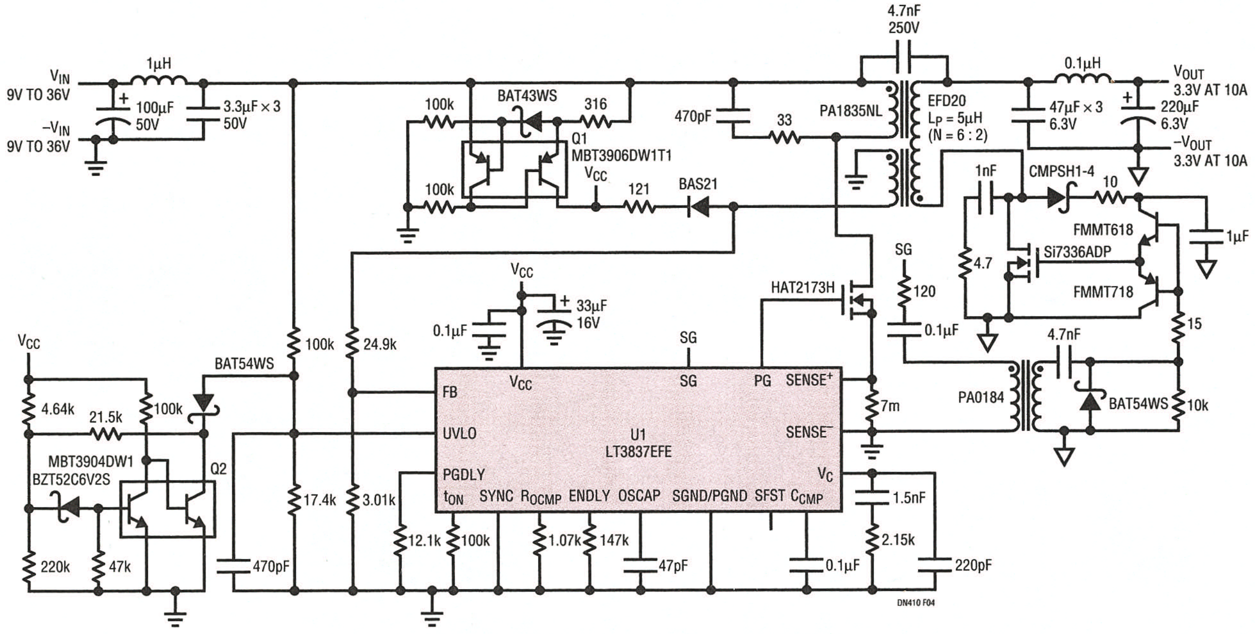

Figure 4. Wide Range, 9V to 36V to 3.3V/10A Isolated Flyback Converter with ±1.2% Regulation

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Single Port PoE

IEEE 802.3af
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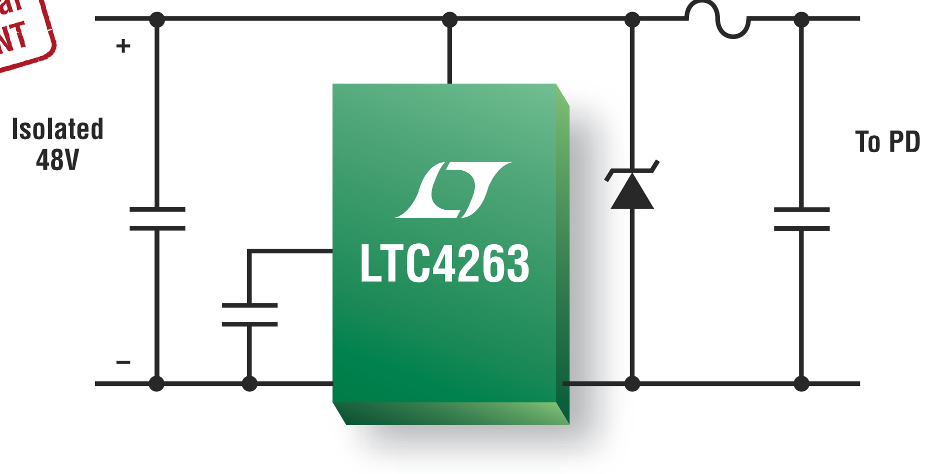

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- Precision Inrush Control with Internal Sense Resistor
- Powered Device (PD) Detection and Classification
- LTC4263: $2.95 each in 1k qty

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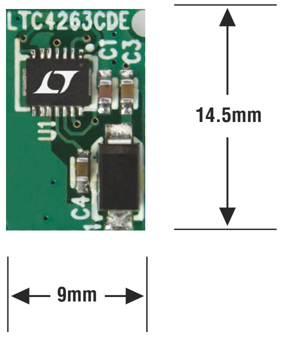

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Single	Dual	Quad	I_{SUPPLY} Max 25°C (µA)	GBW Typ 25°C (kHz)	V_{OS} Max 25°C (µV)	I_{BIAS} Max 0-70°C (nA)	Supply Range (V)
LT6003	**LT6004**	**LT6005**	1	2	500	0.09	1.6 to 16
LT1494	**LT1495**	**LT1496**	1.5	2.7	375	1.2	2.1 to 36
LT1672	**LT1673**	**LT1674**	2	12	375	1.2	2.1 to 36
LT6000	**LT6001**	**LT6002**	16	50	750	5	1.8 to 16

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Current mirror improves PWM regulator's performance

Grant Smith, National Semiconductor, Phoenix, AZ

Power-supply designs requiring high-performance isolated feedback often use an error amplifier similar to the one in **Figure 1**, which relies on a second amplifier, IC_{1B}, to provide the necessary inversion to keep the optocoupler, IC_2, referenced to ground. To prevent bias-supply noise from entering the feedback path and causing oscillations, the amplifier relies on its ground reference and power-supply-rejection characteristics. The power supply's output drives a voltage divider comprising R_1 and R_2 that maintains the amplifier's inverting input at the same voltage as the reference voltage that IC_3 provides. C_2, R_3, and C_3 comprise frequency-compensation components for the power supply's stable operation. This component-intensive error-amplifier configuration requires two operational amplifiers, one precision shunt-voltage reference, four capacitors and often a fifth in parallel with R_6, and seven resistors.

Figure 2 shows an alternative single-amplifier design in which IC_3, an LM4040 precision-voltage reference, drives optocoupler IC_2 with a "stiff" positive-voltage source over a wide current range. The voltage reference suppresses any noise present on the bias-supply rail. Variations in the reference and power-supply voltages appear in common mode at the amplifier's inputs and thus provide additional noise immunity. A resistive-voltage divider comprising R_2 and R_3 reduces the reference voltage to equal the power supply's regulated output voltage, which drives IC_1's inverting input through R_1. Given its single voltage divider, the error-amplifier circuit of **Figure 2** provides the same output voltage as the circuit of **Figure 1** and requires a single operational amplifier and precision shunt reference, four capacitors, and six resistors.

Miller-effect coupling of collector-emitter-voltage transitions into a typical phototransistor-based optocoupler's high-impedance, optically sensitive

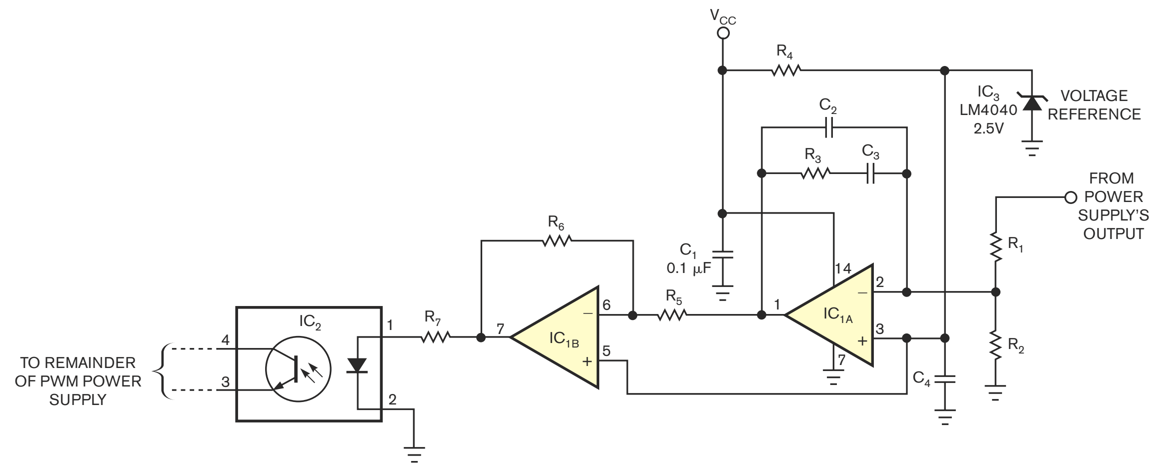

Figure 1 A conventional isolated-feedback circuit requires an extra operational amplifier and adds several passive components to a representative pulse-width-modulated power-supply design.

base region introduces a bandwidth-limiting pole, which dramatically slows the device's response time. Holding the phototransistor's collector-emitter voltage constant and allowing only its collector-emitter current to change provide an order-of-magnitude switching-speed improvement.

National Semiconductor's (www.national.com) LM5026 active-clamp current-mode PWM controller, IC_4, provides a convenient method of reducing an optocoupler's Miller-effect-induced slowdown. **Figure 2** shows the LM5026's internal current mirror driving what would normally serve as a frequency-compensation pin. Optocoupler IC_2 connects directly between two constant-voltage sources comprising the current mirror and a voltage reference. The resultant decrease in response time relocates the bandwidth-limiting pole and improves the circuit's transient response.

The values of C_2, C_3, R_3, and R_1 apply only to this design and may require modification for other applications. Select R_1 to provide equal impedances at both of the op amp's inputs. C_2 forms a high-frequency noise filter. After you measure the converter's overall gain, calculate values for C_3 and R_3 that will provide proper gain and phase response. Several methods of calculation are available, most of which will provide adequate results.**EDN**

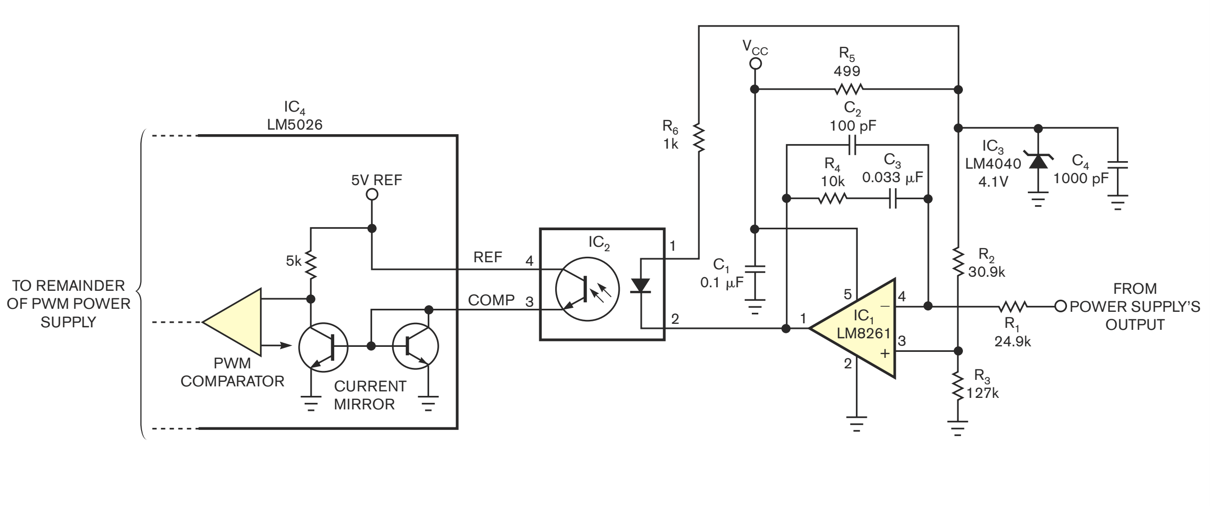

Figure 2 Clamping an optoisolator's voltage excursion improves the PWM-regulator loop's transient response.

Low-cost current monitor tracks high dc currents

Susanne Nell, Breitenfurt, Austria

To measure high levels of direct current for overload detection and protection, designers frequently use either a current-shunt resistor or a toroidal core and Hall-effect magnetic-field sensor. Both methods suffer from drawbacks. For example, measuring 20A with a 10-mΩ resistor dissipates 4W of power as waste heat. The Hall-effect sensor delivers accurate measurements and wastes little power, but it's

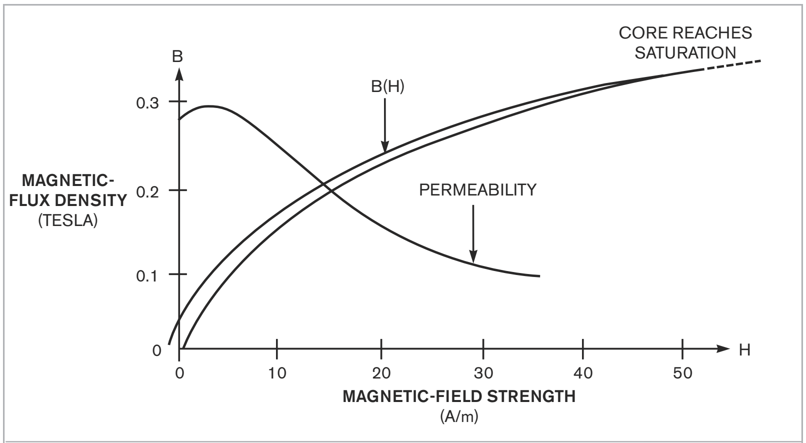

Figure 1 This representative magnetization (BH) curve shows that, as current through an inductor's winding increases, so does magnetizing-field strength, H. When magnetic-flux density, B, can no longer increase, the core's magnetic material has reached saturation.

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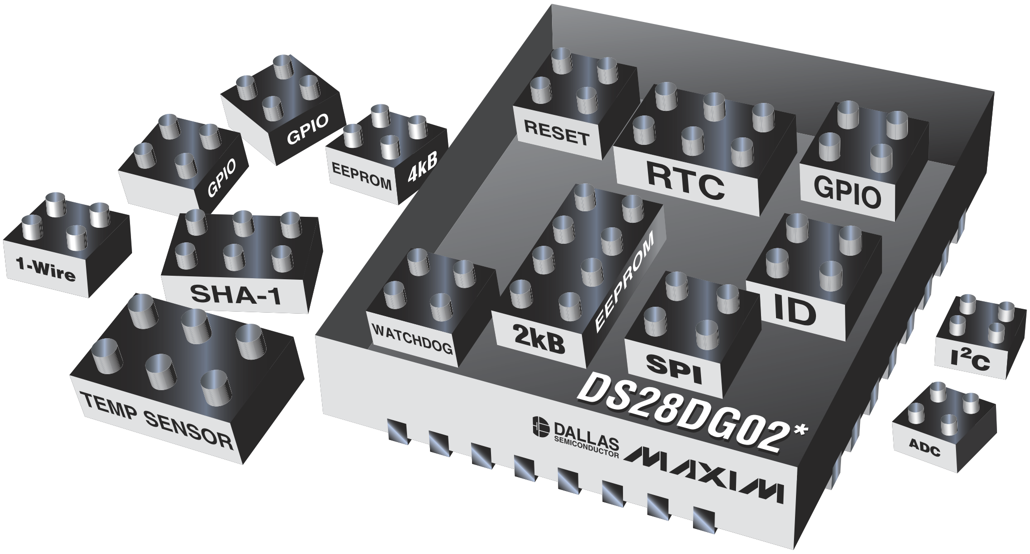

Part	EEPROM (kB)	Interface	No. of Reset Monitors	Real-Time Clock	Temp Sensor	Watchdog Input	GPIOs (Lines)	64-Bit ID	SHA-1 Authentication
DS2431	1	1-Wire®						3	
DS2460	1	I^2C						3	3
DS28CM00		I^2C/SMBus™						3	
DS28CN01*	1	I^2C/SMBus						3	3
DS28CZ04	4	I^2C/SMBus					4		
DS28DG02*	2	SPI™	1	3		3	12	3	
DS28E04-100	4	1-Wire					2	3	
DS28E01-100	1	1-Wire						3	3
DS28EA00*		1-Wire			3		2	3	

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an expensive approach to simple current monitoring.

This Design Idea describes an inexpensive, low-power current-measurement circuit that's useful for measurements of modest accuracy. As a bonus, a filter inductor in a dc/dc converter's input line can double as a current sensor for the measurement circuit. A representative ferrite core's permeability decreases as the core nears saturation (**Figure 1**). The curve's shape and values depend on the core material's characteristics and whether the core includes an air gap.

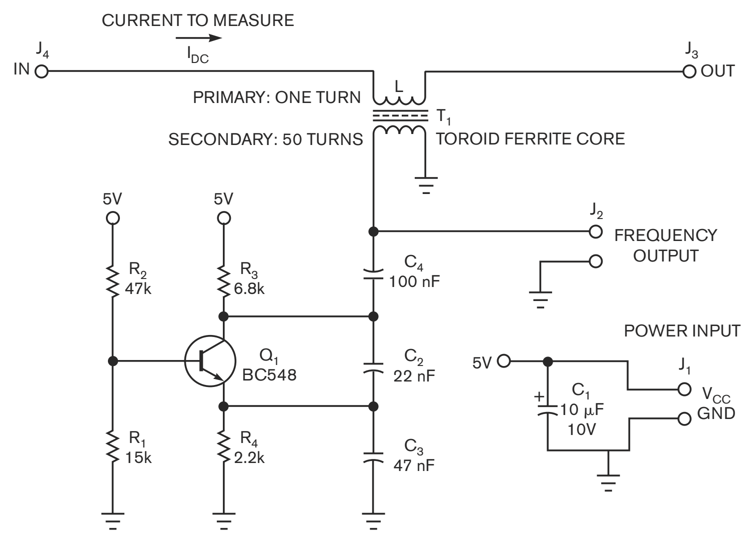

Figure 2 Varying the direct current flowing through the single-turn primary winding alters T_1's secondary winding's inductance, which in turn varies the oscillator's output frequency.

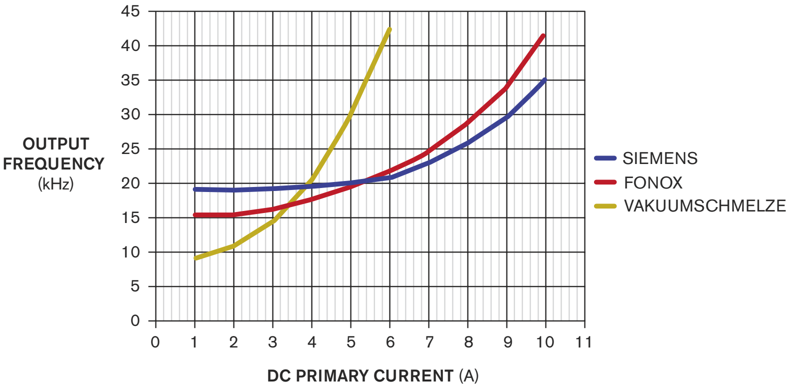

Figure 3 Current-versus-output-frequency plots for three manufacturers' toroidal cores show the influence of the cores' characteristics on frequency linearity and relative sensitivity.

The core's permeability depends on the magnetic-flux level in the ferrite material, which in turn depends on the amount of current flowing through the core's windings. This circuit uses a simple LC oscillator to measure the core's permeability. A primary winding comprising one or more turns wound on the core carries the measurement current. A multiturn secondary winding on the core forms an inductor, L, that determines the oscillator's resonant frequency.

A FILTER INDUCTOR IN A DC/DC CONVERTER'S INPUT LINE CAN DOUBLE AS A CURRENT SENSOR FOR THE MEASUREMENT CIRCUIT.

In theory, any LC oscillator circuit will serve in this application, but, in practice, the current-measurement winding presents a low impedance that damps the LC-tank circuit and causes start-up and stability problems in some oscillator circuits. Of a variety of tested oscillator circuits, the design in **Figure 2** offers the best performance. A number of factors affect the core's permeability, which in turn impacts the circuit's frequency stability and limits its applications to current-overload detection and low-accuracy current measurements.

Figure 3 illustrates the circuit's output-frequency-versus-current characteristics for three vendors' ferrite cores of identical dimensions and number of secondary turns. For best linearity, use a low-hysteresis core material. Cores of virtually any dimensions and materials work in the circuit but require optimization of the number of turns on the oscillator tank and primary windings. Increase the core's air gap, if present, when the current you apply to the core causes saturation before reaching the overload value. For improved performance and linear measurements, use the circuit in a closed-loop configuration (**Reference 1**).**EDN**

REFERENCE

1 Nell, Susanne, "Improved current monitor delivers proportional-voltage output," *EDN*, Jan 19, 2006, pg 84, www.edn.com/article/CA6298271.

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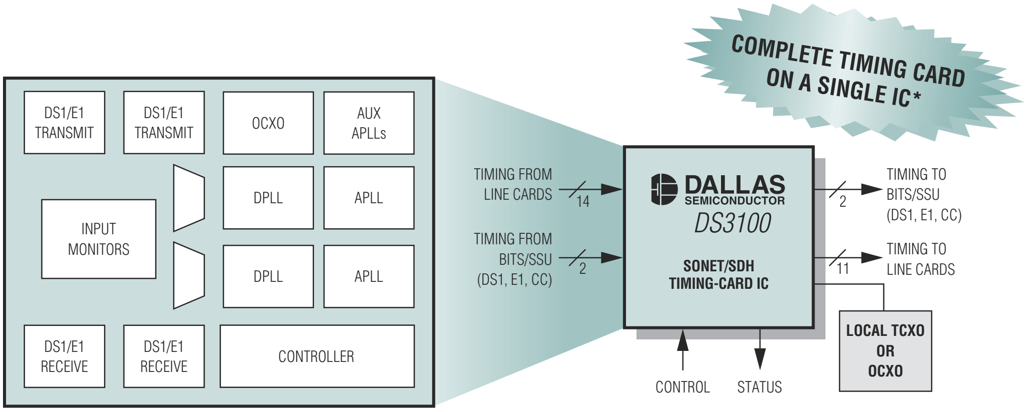

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- ◆ CMOS/TTL and Differential LVDS Outputs Support Rates Up to 311.04MHz
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Digital-I/O circuit adapts to many interface voltages

Steve Hageman, Windsor, CA

To test products in my R&D lab, I build many universal data-acquisition systems that connect to a PC or another controller through RS-232 links or LANs. These small systems typically include multiple ADC, DAC, and digital-I/O channels to control various hardware functions during product design and development. Over the years, I have established a simplified analog-interface standard that spans a 0 to 5V range. On the digital side, many of the newer logic families no longer tolerate 5V inputs and have rendered 5V-only digital-I/O ports obsolescent.

To solve the problem, I designed a flexible digital-interface circuit around a MAX7301 I/O expander from Maxim Integrated Products (www.maxim-ic.com) and a programmable linear-power supply comprising a MAX1658 adjustable linear-voltage regulator under the control of a MAX5400 256-position, digitally programmable potentiometer. This circuit provides a programmable interface matching the logic levels of ICs that require 2.5, 3, 3.3, and 5V power supplies.

Two SPIs (serial-peripheral inter-

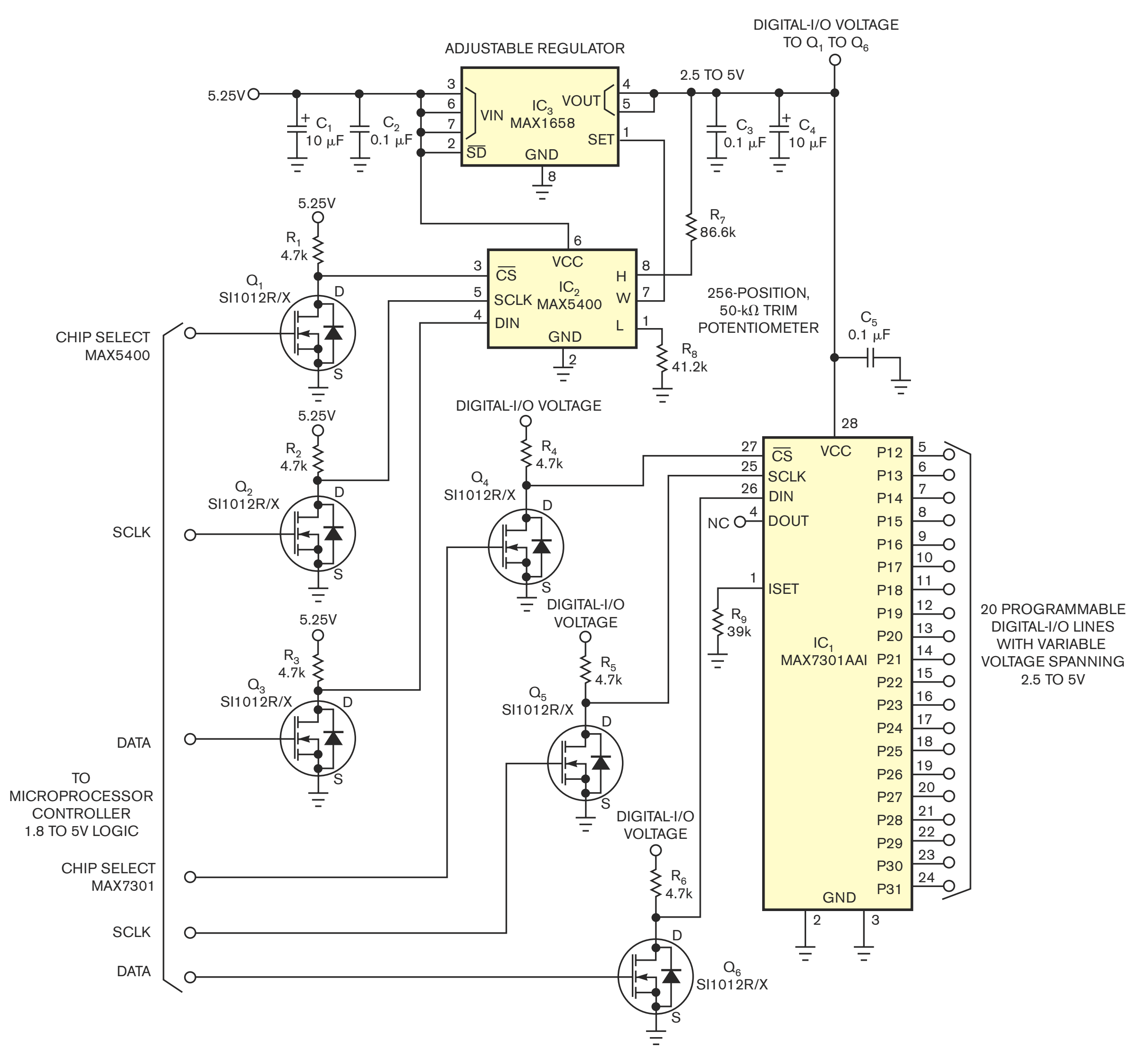

Figure 1 A programmable power supply sets voltage thresholds for a universal digital-I/O device.

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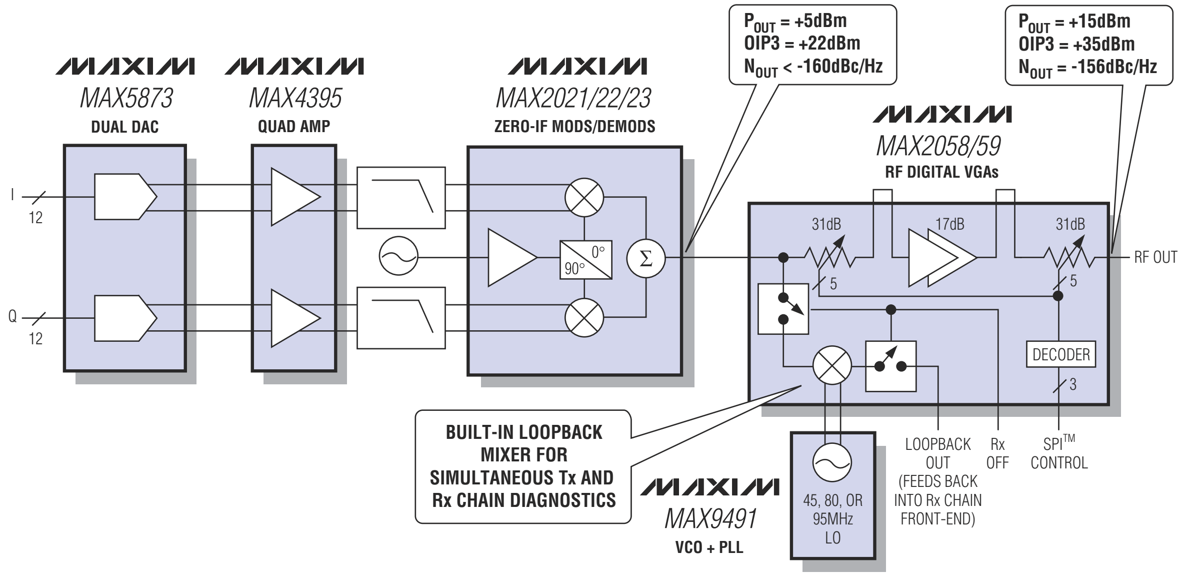

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faces) control all 20 of the MAX7301AAI's input and output pins and voltage thresholds (**Figure 1**). Unlike some SPI-port expanders that include weak, resistor-only pullups, the MAX7301, IC$_1$, features true, active-pullup, "totem-pole" outputs that can source higher currents. When powered by the SPI-programmable linear regulator, the MAX7301's outputs can deliver logic levels of 2.5 to 5V. The programming interfaces for both devices comprise two three-wire (plus ground) SPI connections that use only six of the controller's signal lines.

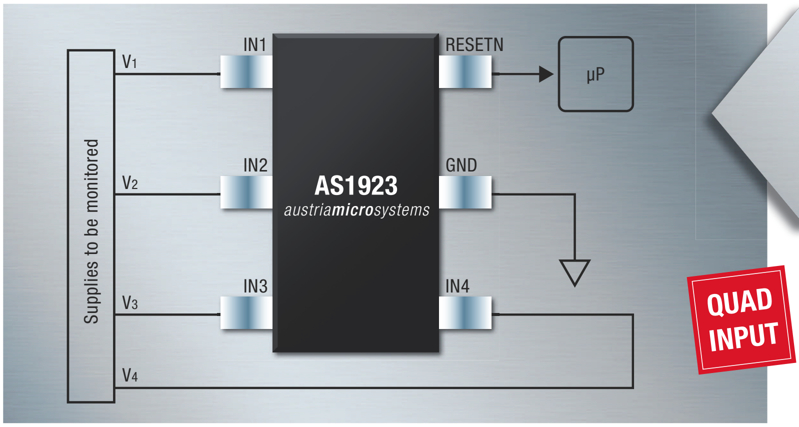
Six Vishay (www.vishay.com) Si1012R low-gate-voltage-threshold N-channel MOSFETs, Q$_1$ through Q$_6$, isolate the controllers' fixed-output-voltage levels from IC$_1$'s variable-input-threshold voltages. Although any of several IC-level-translator ICs work equally well, the inexpensive MOSFET buffers occupy small footprints on the interface's PCB (printed-circuit board). For operation at serial-interface clock rates approaching IC$_1$'s 26-MHz maximum, optimize the values of resistors R$_1$ through R$_6$ to provide adequate rise times at the selected clock rate. These values are adequate for operation at the 1-MHz SPI clock rate that a low-power microcontroller produces.

UNLIKE SOME SPI-PORT EXPANDERS THAT INCLUDE WEAK, RESISTOR-ONLY PULLUPS, THE MAX7301, IC$_1$, FEATURES TRUE ACTIVE-PULLUP, "TOTEM-POLE" OUTPUTS THAT CAN SOURCE HIGHER CURRENTS.

To alter the circuit's output-voltage level, IC$_2$, a 256-step Maxim MAX5400 digital potentiometer, controls IC$_3$, a Maxim MAX1658 adjustable-voltage linear regulator. Writing all zeros to IC$_2$ sets IC$_3$'s output voltage to slightly more than 5V, and writing all ones (255 decimal) to IC$_2$ reduces IC$_3$'s output voltage to slightly less than 2.5V. To compensate for component tolerances, the circuit provides enough voltage overrange to cover the full 2.5 to 5V range. Writing 128 (decimal) to IC$_2$ should produce a nominal 3.25V output. Measure IC$_3$'s actual output voltage and subtract it from the nominal voltage to produce an offset count for calibration correction.

In operation, the host controller sets IC$_3$'s regulated output voltage through IC$_2$ and determines the maximum voltages of IC$_1$'s logic inputs and outputs. Next, the controller configures IC$_1$'s inputs and outputs as necessary for the interface task at hand. The MAX7301's standard CMOS logic-threshold voltages of 0.3 to 0.7 times its supply voltage for low and high inputs, respectively, interface with other CMOS parts. **EDN**

AS1923 - Quad Voltage Supervisor



- 1.0 to 5.5V Supply Voltage
- Quad Sense - Single Reset
- Adjustable or Fixed Thresholds
- Small SOT23 package

The AS1923 allows to pull a single reset if one of its four supervised inputs goes below a certain threshold.

Ideal for multi-supply applications where small size and performance are critical as in FPGA and DSP based intelligent instruments and any critical CPU monitoring.

Part No.	Thresholds (16 variants)				Supply	Supply Current	Package
	V(1)	V(2)	V(3)	V(4)	V	µA (typ)	
AS1923	5, Adj	3.0, 3.3	2.5, 1.8, Adj	-5, 1.8, Adj	1.0 to 5.5	55	SOT23-6

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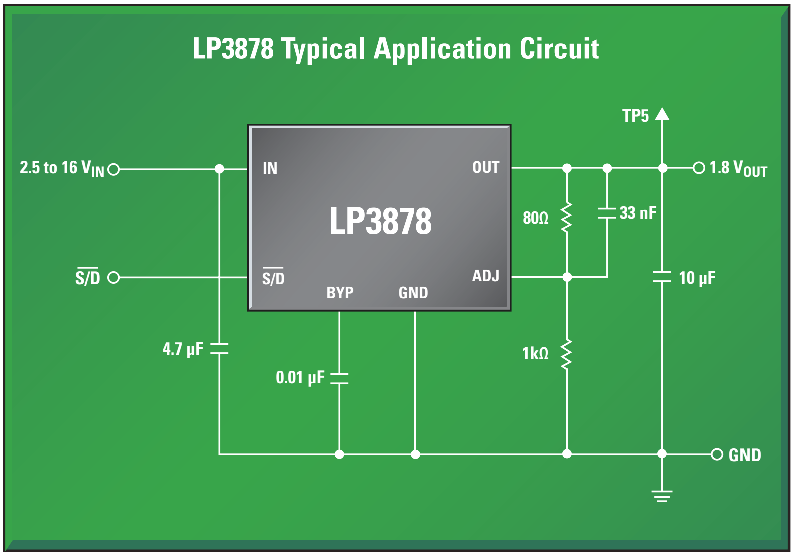
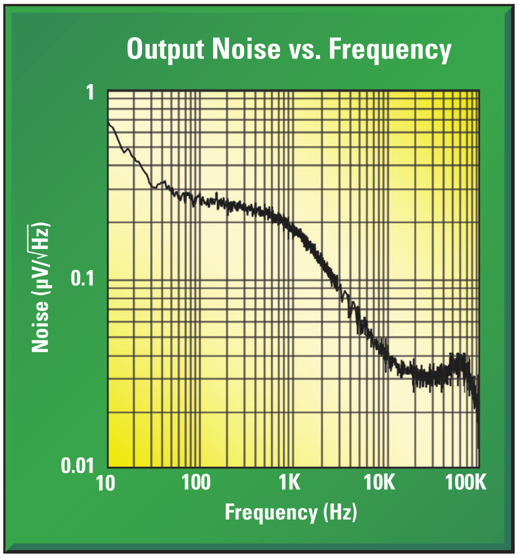

LP3878 Typical Application Circuit


Output Noise vs. Frequency

Product ID	V_{IN}	V_{OUT}	Load	Output Noise	Package
LP3878	2.5V to 16V	ADJ (1.0 to 5.5V)	800 mA	18 μV	PSOP-8, LLP-8
LP3879	2.5V to 6V	1.0, 1.2V	800 mA	18 μV	PSOP-8, LLP-8
LP5900	2.5V to 5.5V	1.5V to 3.3V	100 mA	6.5 μV	micro SMD-4, LLP-6

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productroundup

POWER SOURCES

Power-supply series increases dc-output-voltage range

Expanding the vendor's line of modular DIN-rail-mounted power supplies, CSF power supplies now include units providing 5V dc at 8A, 12 to 15V dc at 6 and 8A, 24V dc at 3 and 5A, and 48V dc at 2.5A. The devices feature autoranging at 90 to 264V-ac input, suiting international applications and short-circuit, overload, and overtemperature protection. Prices for the CSF power supplies range from $95 to $300.

Automation Systems Interconnect, www.asi-ez.com

300W BCM runs at high efficiency

Claiming greater than 95% efficiency, the B352F110T30 BCM (bus-converter module) SAC (sine-amplitude converter) operates from a 330 to 365V-dc primary bus, delivering an isolated 10.3 to 11.4V secondary. This isolated, 11 to 352V, 300W converter suits high-voltage distribution systems, ac/dc switched-mode power supplies, and RF amplifiers. The device has a 1000W/in.^{3} power density. Measuring 1.28×0.87×0.26 in., the B352F110T30 BCM costs $37.40.

Vicor Corp, **www.vicr.com**

Front-end/rectifier series has an onboard microcontroller

The front-end/rectifier CAR-2500 1U, 2500W power-supply series provides 27W/in.^{3} and 92% efficiency. An onboard microcontroller with a 10-bit ADC allows for a more accurate temperature, current, and

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Eighth Brick

Our E48SH and E48SR, 36V-75V input, single output, isolated DC/DC converters, delivers up to 50A or 120 Watts of power in an Industry Standard eighth brick form factor and pin-out.

Product	Vin	Vout	Iout(Max)	Power(Max)	Efficiency
E48SR	36V ~ 75V	1.2V ~ 15V	25A	84W	Up to 93%
E24SR	18V ~ 36V	3.3V ~ 12V	20A	66W	Up to 92%
E48SH	36V ~ 75V	1.2V ~ 12V	50A	120W	Up to 93.5%

Sixteenth Brick

Our V48SR, 36-75V input, single output, isolated converters are available in an Industry Standard form factor and pin-out, (1.3"x 0.90"), while offering up to 25A or 66 Watts of output power!

Product	Vin	Vout	Iout (Max)	Power (Max)	Efficiency
V48SR	36V~75V	1.2V~15V	25A	66W	Up to 91%

Both of these units offer amazing flexibility and power density for even the most space constrained and cost-sensitive applications.

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POWER SOURCES

voltage-sensing capability. Additional features include an I^{2}C, a PMBus, and Ethernet protocols. Delivering 54V dc at 46.3A for high-line operations of 230V ac, the device has a standby voltage of 3.3 or 5V at 1A to power external housekeeping and monitoring circuitry. Able to fit four units side by side in a 1U power shelf, the series supplies as much as 10,000W or 7500W N+1 redundant power. Measuring 1.61×4×14.25 in., the CAR2500 front-end/rectifier series costs $399.

Cherokee International, www.cherokeepwr.com

Power shelf allows hot docking and removal

Able to accommodate three D1U power supplies, the 1U-high, 19-in. S1U-3X power shelf requires no custom chassis. The device allows hot docking and removal of power supplies and features a blind-docking connection. The 12V version holding three D1U-W-1600-12 power supplies supports 4.8 kW of bulk 12V power, and the 48V version containing three D1U-W-2000-48 power supplies supports 6 kW of bulk 48V power. The S1U-3X power shelf costs $428.76 (100).

C&D Technologies, www.cd4power.com

DIN-rail power supplies have regulated, adjustable output voltages

Available in 14 models, the Tracopower TSP DIN-rail power-supply series offers add-on-function modules providing battery backup, output buffering, or true redundant operation in system applications. The devices come in regulated, adjustable 12, 24, or 48V-dc output voltages with 25A ratings. Providing thermal-overload protection, the power supplies have a −25 to +70°C temperature range with convection cooling. Including a standard remote on/off feature, the TSP costs $71.50 (100).

Power Sources Unlimited, www.psui.com

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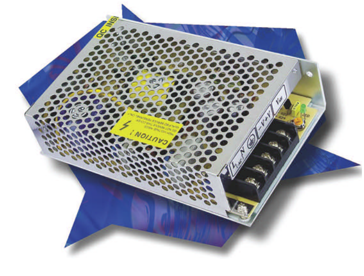
productroundup

POWER SOURCES

Single-output power supplies are CE-certified

Operating from an 85 to 264V universal ac-input range, the HF60W-SL enclosed compact ac/dc power-supply family provides 60W single outputs of 5, 12, 15, 24, and 48V dc. Features include a 0.5% tight line/load regulation, 3000V-ac I/O isolation, and 20-msec holdup time. The HF60W-SL power supplies have EN60850 approval and CE certification, and they cost $28.45.



MicroPower Direct, www.micropowerdirect.com

External power supply suits medical and industrial applications

Providing Class II system protection, the PDM60 external ac/dc power supply has UL609501 and EN609501 safety approvals for industrial and IT applications, and UL60601-1 and EN60601-1 approvals for medical systems. Class II systems require no grounded ac-input socket for normal operation, compared with Class I systems, which rely on insulation and an earth connection for protection. Suiting portable applications, the power supply measures 135×65×41 mm. The PDM60 costs $40.30 (1000).

XP Power, www.xppower.com

EDA TOOLS

Verilog 2001 simulator provides faster RTL and gate-level simulations

Reducing simulation-debugging time, the compiled-code VeriLogger Extreme Verilog 2001 simulator provides fast simulation of RTL and gate-level simulations using SDF (Synopsys Delay Format) timing information. VeriLogger Extreme claims eight-times-faster RTL simulation and 30-times-faster gate-level simulation than VeriLogger Pro. The simulator supports design libraries and design flows for all major ASIC and FPGA vendors and comes bundled with the vendor's BugHunter Pro graphical Verilog/VHDL integrated development environment. Suiting low-memory usage, the product allows large designs to run on memory-constrained laptops. VeriLogger Extreme is available on Linux, Solaris, and Windows; a perpetual license costs $4000 on Windows, with a 24% discount through March 2007. Current VeriLogger Pro customers with maintenance contracts can upgrade for free.

SynaptiCAD, www.syncad.com

Processor designer supports next-generation VLIW processors

The most recent release of the vendor's Processor Designer uses the most recent extensions in the open LISA (Language for Instruction Set Architectures). LISA increases support for next-generation VLIW (very-long-instruction-word) processors, an optimal target for current C-compiler technology. The product automates the exploration of the number of parallel VLIW slots with the generation of the software-development tools, such as an assembler, a linker, a simulator, and a C compiler for software-performance measurement, as well as RTL-code generation for hardware-cost estimation. Prices for the most recent version of Processor Designer range from $150,000 to $300,000.

CoWare, www.coware.com

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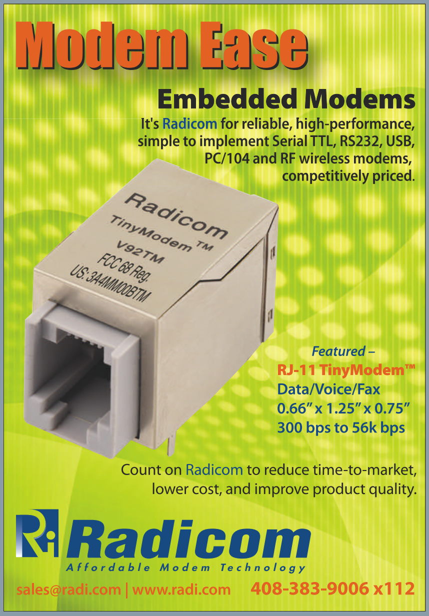
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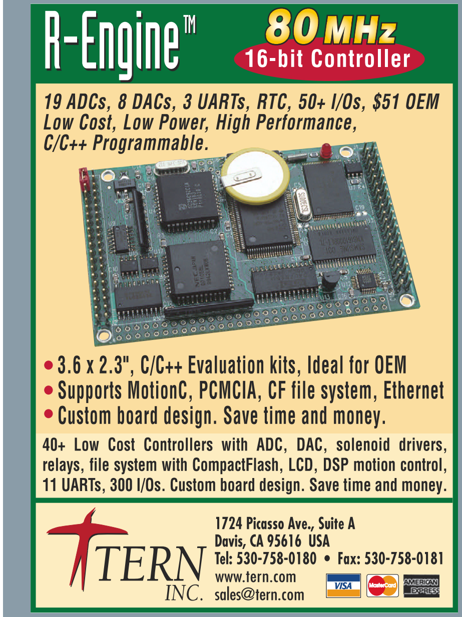
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scope

CHART YOUR COURSE

LOOKING AHEAD

TO PRESIDENTS' DAY AT CTIA WIRELESS 2007

If you have any doubt that the convergence of information, communications, and media onto wireless devices has the attention of the rich and powerful, check out the CTIA (Cellular Telecommunications and Internet Association). Billed as "the world's largest convergence marketplace" on its humble Web site, CTIA Wireless 2007 thunders to life March 25 through 29 at the Orange County Convention Center in Orlando, FL. Keynote speeches will include Microsoft, AT&T, and Motorola executives comparing notes on wireless convergence and chief executive officers from Orange Group, Visa USA, Viacom, and EMI Group exchanging views on emerging opportunities in the wide-open race to exploit convergence platforms. However, the planned joint appearance of former US Presidents George HW Bush and Bill Clinton giving their executive perspective on the industry will upstage all these presentations. Oh yes, and there will be technical sessions, too.

LOOKING BACK

TO THE ULTIMATE SUPER-TWEETER

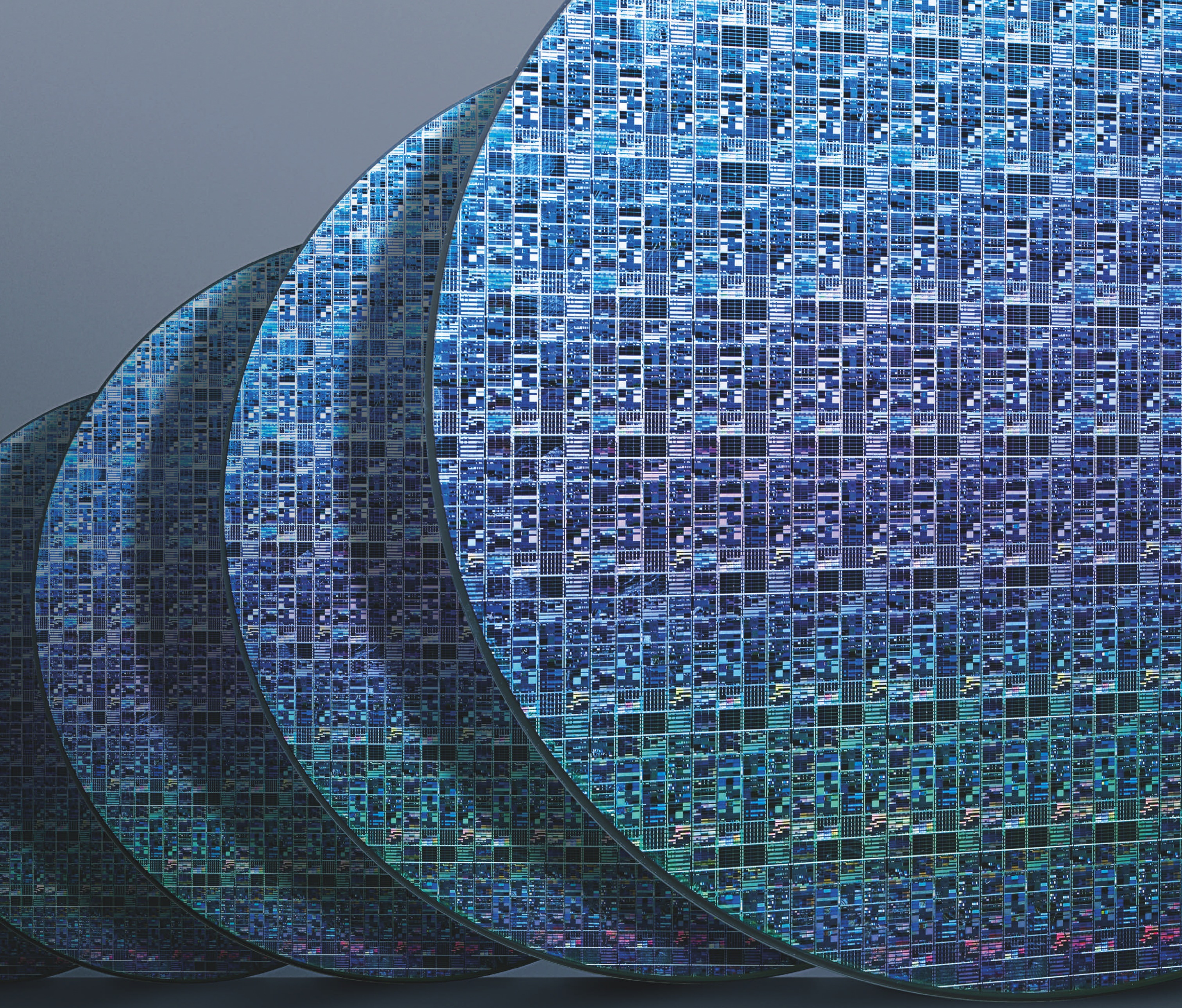
An expanding and contracting ionic cloud of air within a miniature quartz cell produces sound waves, offering extremely high-fidelity reproduction when used in place of a loudspeaker diaphragm. The heart of the device is an open-ended quartz cell nearly as large as a peanut shell, enclosing a chamber that tapers to an aperture about the size of an automatic pencil lead. A high-voltage, high-frequency current ionizes the air within the cell. A second electric field produces expansion and contraction of the ionized cloud, resulting in sound waves. Termed Ionovac by its producer the DuKane Company, the cell is a greatly improved version of the Ionophone principle invented several years ago in Europe. DuKane developed the device to be a flexible generator of both audible and ultrasonic waves and will offer it initially to the high-fidelity market as a loudspeaker.

—*Electrical Design News*, March 1957

LOOKING AROUND

AT A CHANGING DRAM MARKET

At this point, it's clear that no one is stampeding to get Microsoft Vista. Corporate IT departments are, as industry pundits predicted, waiting, and the initial response from consumers has been modest. This response suggests that the impact of the new operating system will be primarily on consumers' and small businesses' PC purchases, rather than on wholesale upgrades or replacements of masses of machines. And that scenario suggests that a tight market for PC-memory modules isn't in the cards for early 2007. This could make PC memory a bargain for other applications—worth a look even if it means changing some design specifications.



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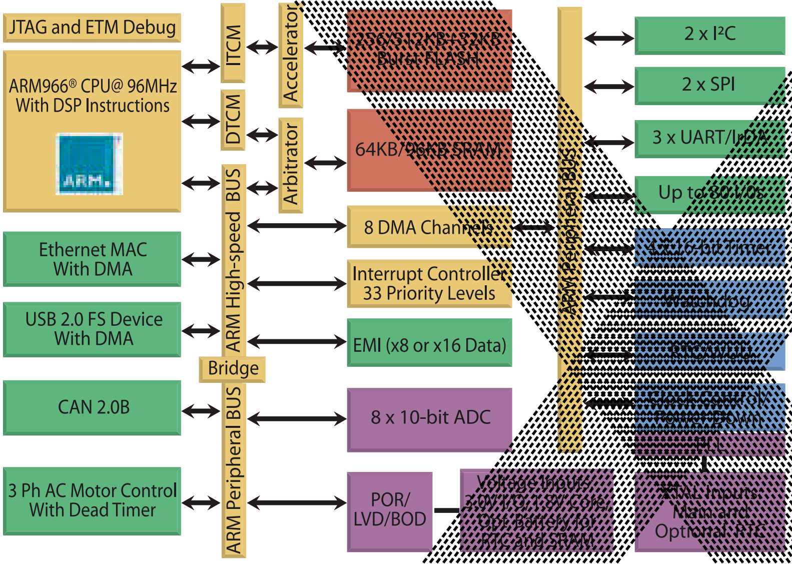

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STR910FW32X	256 + 32	64	8x10-bit				80 (16)	LQFP128		CAN, EMI
STR911FM42X	256 + 32	96	8x10-bit				40 (16)	LQFP80		USB, CAN
STR911FM44X	512 + 32	96	8x10-bit				40 (16)	LQFP80		USB, CAN
STR912FW42X	256 + 32	96	8x10-bit				80 (16)	LQFP128		Ethernet, USB, CAN, EMI
STR912FW44X	512 + 32	96	8x10-bit				80 (16)	LQFP128		Ethernet, USB, CAN, EMI

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